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Model Name : P7YE0/P7YH0/P7YS0

File Name : LA-6911P

BOM P/N:43

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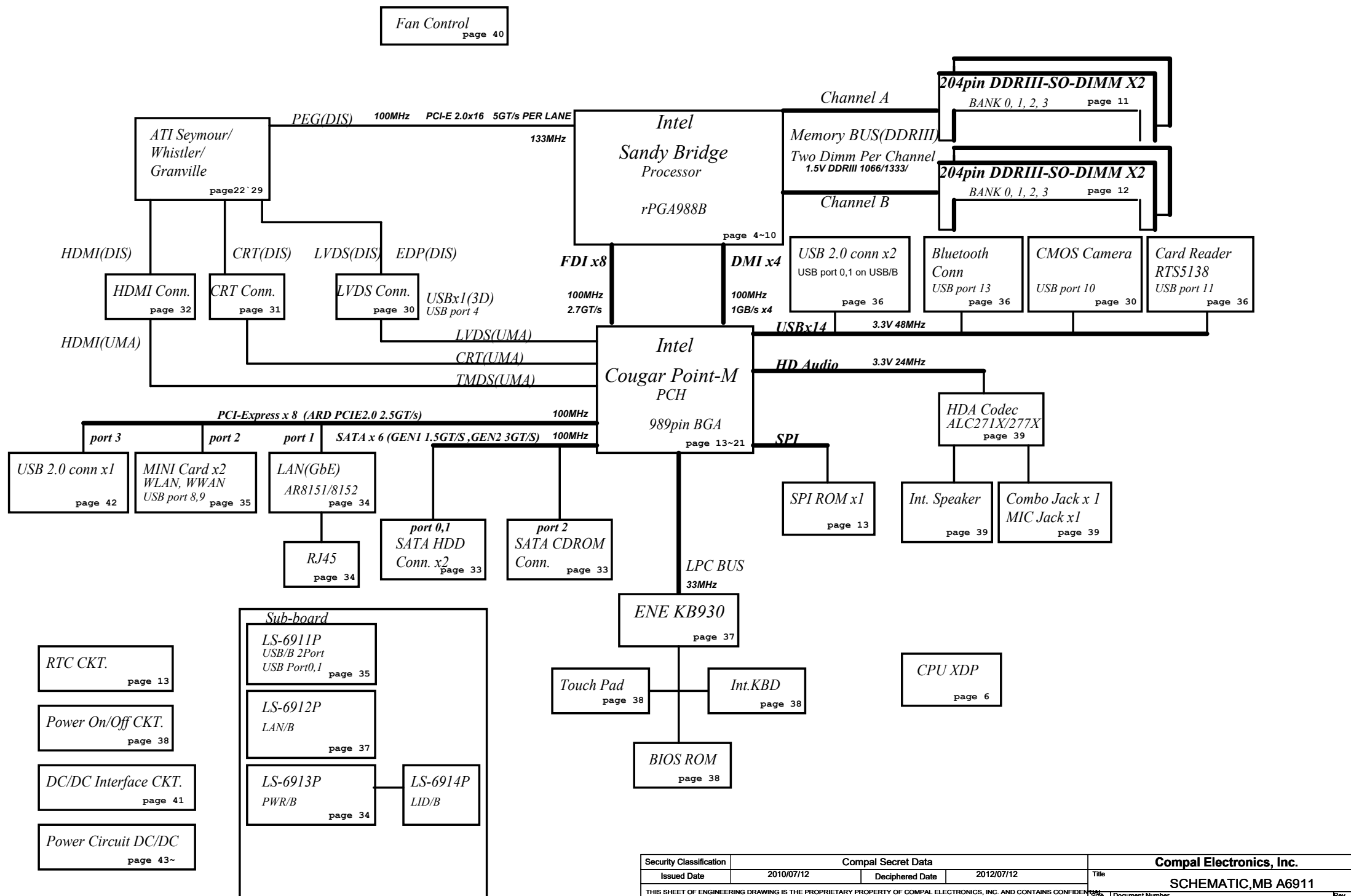
P7YE0/P7YH0/P7YS0 M/B Schematics Document

Intel Sandy Bridge Processor with DDRIII + Cougar Point PCH
ATI Seymour/Whistler/Granville

2010-11-01

REV: 0.3

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Fan Control
page 40

Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
BATT+	Battery power supply (12.6V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+VGA_CORE	Core voltage for GPU	ON	OFF	OFF
+VGFX_CORE	Core voltage for UMA graphic	ON	OFF	OFF
+0.75VS	+0.75VP to +0.75VS switched power rail for DDR terminator	ON	OFF	OFF
+1.0VSDGPU	+1.0VSDGPU switched power rail for GPU	ON	OFF	OFF
+1.05VS_VTT	+1.05VS_VTTP to +1.05VS_VTT switched power rail for CPU	ON	OFF	OFF
+1.05VS_PCH	+1.05VS_VTT to +1.05VS_PCH power for PCH	ON	OFF	OFF
+1.5V	+1.5VP to +1.5V power rail for DDRIII	ON	ON	OFF
+1.5VS	+1.5V to +1.5VS switched power rail	ON	OFF	OFF
+1.5VSDGPU	+1.5V to +1.5VSDGPU switched power rail for GPU	ON	OFF	OFF
+1.8VS	(+5VALW or +3VALW) to 1.8V switched power rail to PCH & GPU	ON	OFF	OFF
+3VALW	+3VALW always on power rail	ON	ON	ON*
+3VALW_PCH	+3VALW to +3VALW_PCH power rail for PCH (Short Jumper)	ON	ON	ON*
+3VS	+3VALW to +3VS power rail	ON	OFF	OFF
+5VALW	+5VALWP to +5VALW power rail	ON	ON	ON*
+5VALW_PCH	+5VALW to +5VALW_PCH power rail for PCH (Short resister)	ON	ON	ON*
+5VS	+5VALW to +5VS switched power rail	ON	OFF	OFF
+VSB	+VSBP to +VSB always on power rail for sequence control	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON
Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.				

EC SM Bus1 address

EC SM Bus2 address

Device	Address	Device	Address
Smart Battery	0001 011X b		

PCH SM Bus address

Device	Address	VRAM P/N
ChannelA DIMM0 A0	1010 000X JDIMM1	SAM 64*16 900M SA00004GS10(S IC D3 64M16 K4W1G1646G-BC11 FBGA ABOI)
		SAM 64*16 800M SA000035720(S IC D3 64MX16 K4W1G1646E-HC12 FBGA ABOI)
DIMM1 A2	1010 001X JDIMM3	SAM 128*16 800M SA00003M060 (S IC D3 128M16 K4W2G1646C-HC12 FBGA ABOI)
		HYN 64*16 900M SA000041S40(S IC D3 64MX16 H5TQ1G63DFR-11C FBGA ABOI)
ChannelB DIMM0 A4	1010 010X JDIMM2	HYN 64*16 800M SA000032420 (S IC D3 64MX16 H5TQ1G63BFR-12C FBGA ABOI)
		HYN 128*16 800M SA00003VS10 (S IC D3 128M16 H5TQ2G63BFR-12C FBGA ABOI)
DIMM1 A6	1010 011X JDIMM4	HYN 64*16 800M SA0000324G0(S IC D3 64M16 H5TQ1G63DFR-12C FBGA ABOI)

BT Config	GPU config	BACO config
BT SKU: BT@	Whistler: WHIS@	BACO: BACO@
4DIMM config	Seymour: SEYM@	nonBACO: NOBACO@
4 DIMM: 4DIMM@	Granville: GRAN@	Muxless config
LVDS/eDP config	Granville config	Muxless: MUXL@
UMA LVDS: ULVDS@	Granville: GRAN@ (VDDCI)	nonMuxless: NOMUXL@ (DISO,UMAO)
DIS LVDS: DLVDS@	nonGranville: NOGRAN@ (VGA_CORE)	VRAM BOM Config
DIS eDP: DEDP@	GPU Frame config	X76264BOL01: 64Mx16x4 Seymour 512M HYN NEW
	128bit: 128@ (WHIS,GRAN)	X76264BOL02: 64Mx16x4 Seymour 512M HYN OLD
		X76264BOL03: 64Mx16x8 Whistler/Granville 1G HYN NEW
		X76264BOL04: 64Mx16x8 Whistler/Granville 1G HYN OLD
		X76264BOL05: 128Mx16x8 Whistler/Granville 2G HYN
		X76264BOL06: 128Mx16x8 Whistler/Granville 2G SAM
		X76264BOL07: 128Mx16x4 Seymour 1G SAM
		X76264BOL08: 128Mx16x4 Seymour 1G HYN

BOM Config		
* UMA Only LVDS Panel:	BT@/UMAO@/UMA@/ULVDS@/NOMUXL@	+DIMM,USB option
* DIS Only LVDS Panel:	BT@/DIS@/VGA@/DISO@/DLVDS@/NOMUXL@	+DIMM,USB option
DIS Only EDP Panel:	BT@/DIS@/VGA@/DISO@/DEDP@/NOMUXL@	+DIMM,USB option
* Muxless BACO LVDS Panel:	BT@/UMA@/DIS@/VGA@/ULVDS@/BACO@/MUXL@	+DIMM,USB option
Muxless nonBACO LVDS Panel:	BT@/UMA@/DIS@/VGA@/ULVDS@/NOBACO@/MUXL@ +X76+GPU(G)	+DIMM,USB option

STATE	SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)		LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)		LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%			
Ra/Rc/Re	100K +/- 5%			
Board ID	Rb / Rd / Rf	VAD_BID min	VAD_BID typ	VAD_BID max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

BOARD ID Table

Board ID	PCB Revision
0	0.1
1	0.2
2	0.3
3	1.0
4	
5	
6	
7	

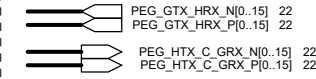
USB Port Table

USB 2.0	USB 1.1	Port	3 External USB Port
EHCI1	UHCI0	0	USB/B(Right side 2.0 option)
		1	USB/B(Right side 2.0 option)
	UHCI1	2	USB port(left side 2.0)
		3	USB/B(Right side 3.0 option)
	UHCI2	4	
		5	
EHCI2	UHCI3	6	
		7	
	UHCI4	8	Mini Card(WLAN)
		9	Mini Card
	UHCI5	10	Camera
		11	Card Reader
	UHCI6	12	
		13	Blue Tooth

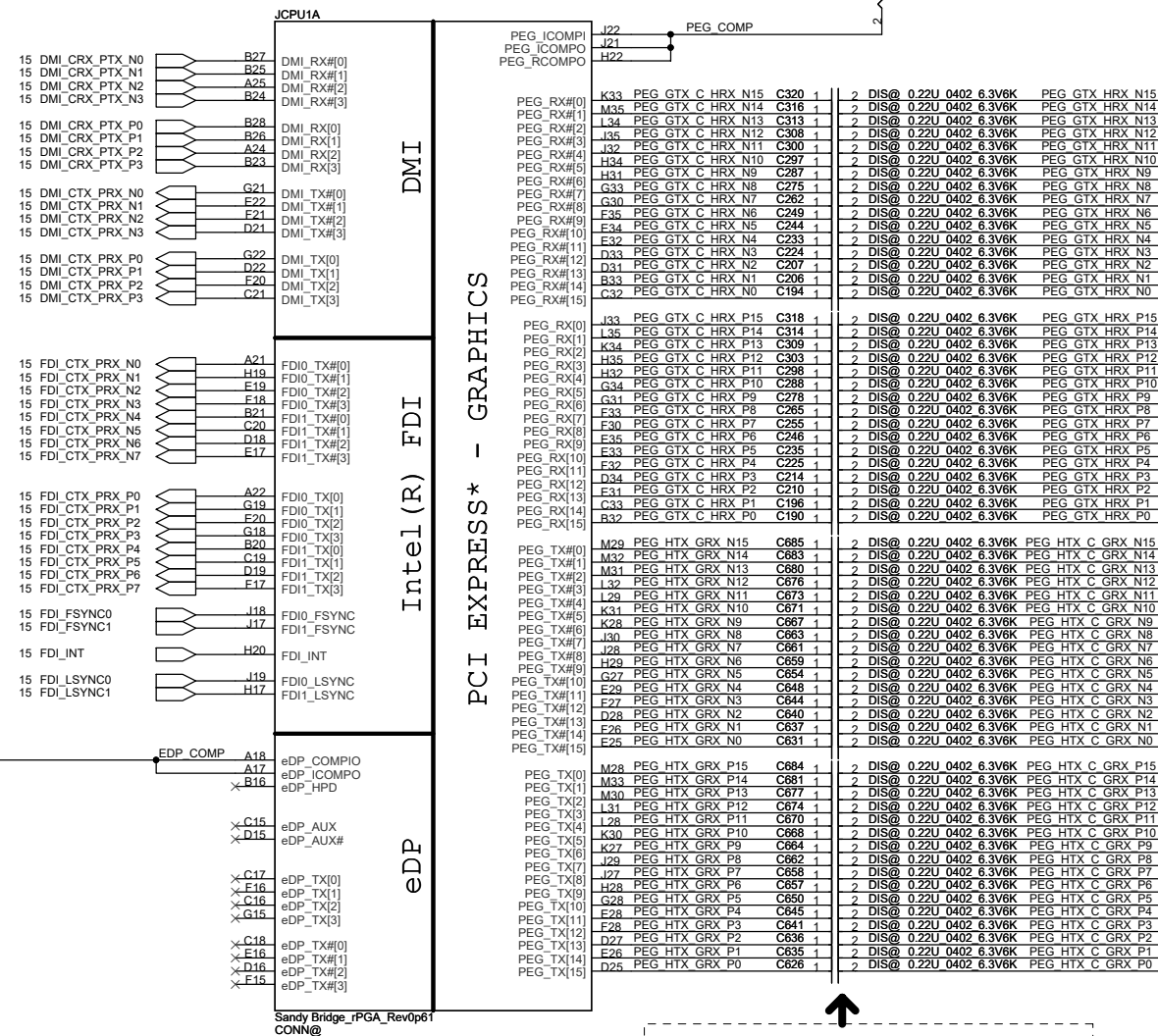
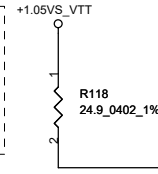
BTO Item	BOM Structure
UMA Only	UMAO@
Muxless/UMA	UMA@
DIS Only	DISO@
Muxless/DIS	DIS@
Muxless/DIS	VGA@
BACO mode	BACO@
nonBACO mode	NOBACO@
VRAM	X76@
128bit VRAM	128@
Granville GPU	GRAN@
Whistler GPU	WHIS@
Seymour GPU	SEYM@
non Granville GPU	NOGRAN@
Blue Tooth	BT@
Connector	CONN@
Unpop	@
DIS eDP	DEDP@
UMA LVDS	ULVDS@
DIS LVDS	DLVDS@
Muxless	MUXL@
non Muxless	NOMUXL@
USB2.0 Conn	USB2@
USB3.0 Conn	USB3@
4 Dimm	4DIMM@

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PEG_ICOMPI and RCOMPO signals should be shorted and routed with - max length = 500 mils - typical impedance = 43 mohms
PEG_ICOMPO signals should be routed with - max length = 500 mils - typical impedance = 14.5 mohms



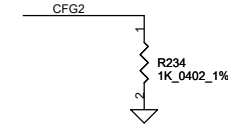
eDP_COMPIO and ICOMPO signals should be shorted near balls and routed with typical impedance <25 mohms
should not be left floating ,even if disable eDP function...



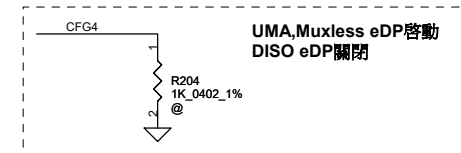
Typ- suggest 220nF. The change in AC capacitor value from 100nF to 220nF is to enable compatibility with future platforms having PCIe Gen3 (8GT/s)

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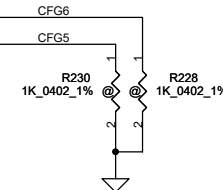
CFG Straps for Processor



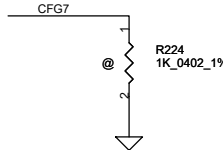
PEG Static Lane Reversal - CFG2 is for the 16x	
CFG2	1: Normal Operation; Lane # definition matches socket pin map definition * 0: Lane Reversed



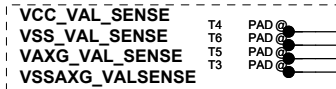
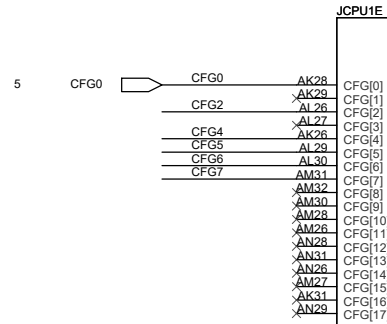
eDP enable	
CFG4	* 1: Disable 0: Enable



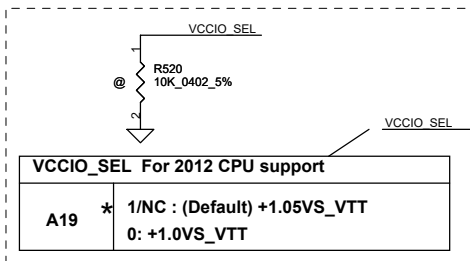
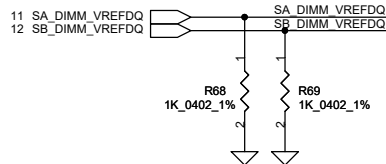
PCIe Port Bifurcation Straps	
CFG[6:5]	*11: (Default) 1x16 PCI Express 10: 2x8 PCI Express 01: Reserved 00: 1x8,2x4 PCI Express



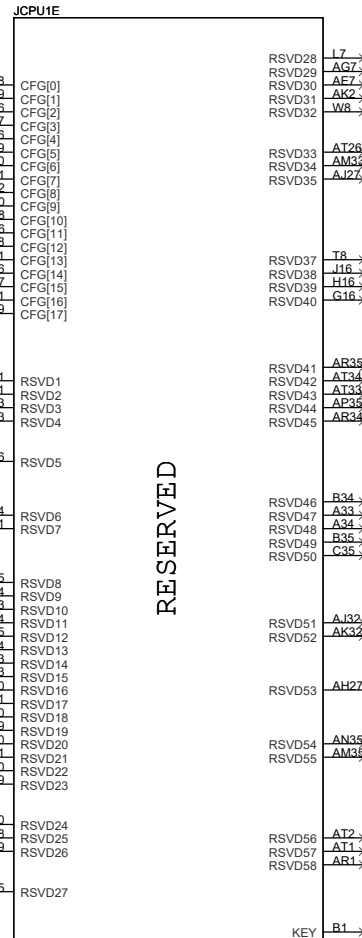
PEG DEFER TRAINING	
CFG7	1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training



SA_DIMM_VREFDQ
SB_DIMM_VREFDQ
 For Future CPU M3 support,
 Sandy bridge not support M3,
 Check list 1.0 & CRB say can NC



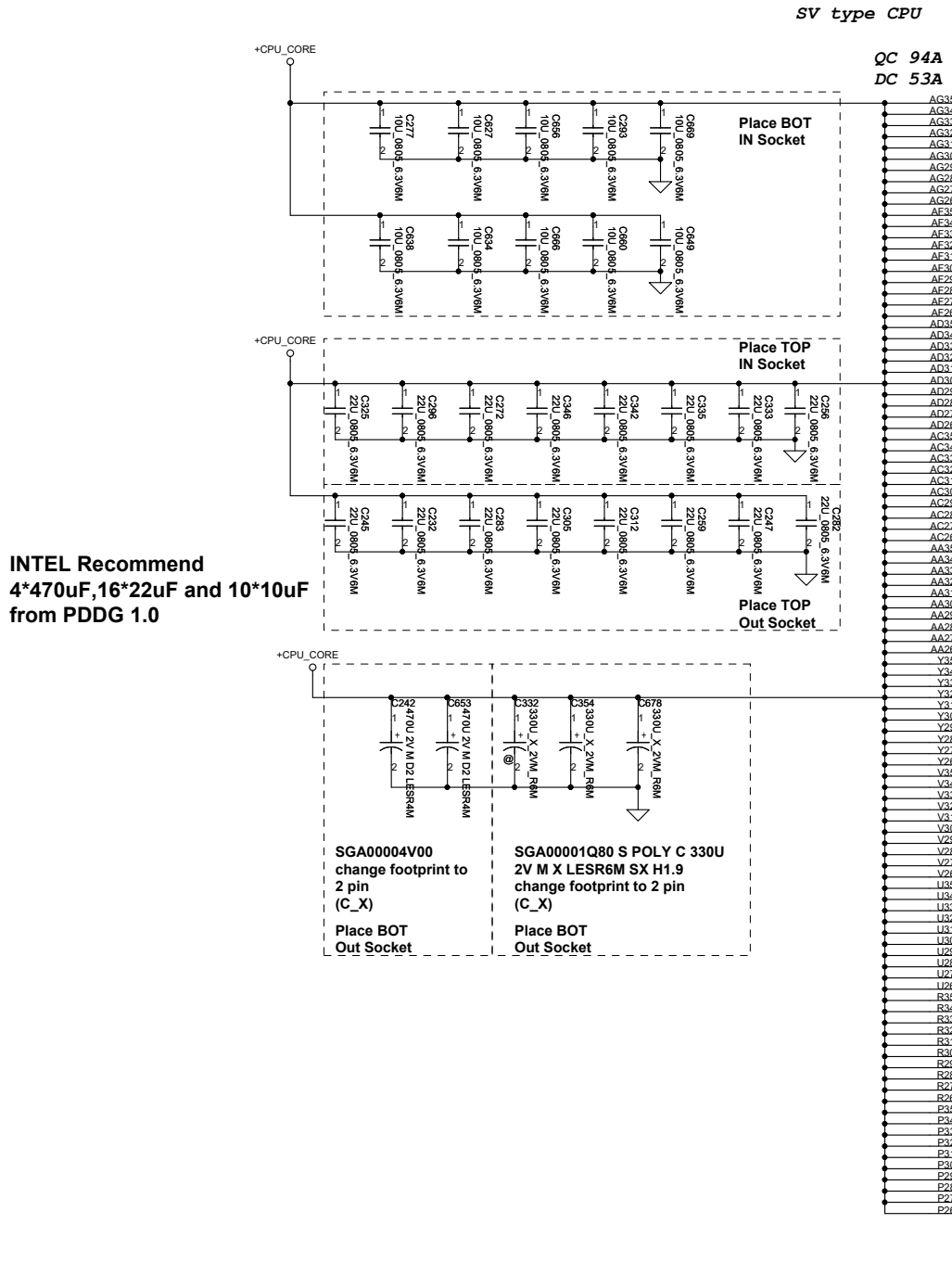
VCCIO_SEL For 2012 CPU support	
A19	* 1/NC : (Default) +1.05VS_VTT 0: +1.0VS_VTT



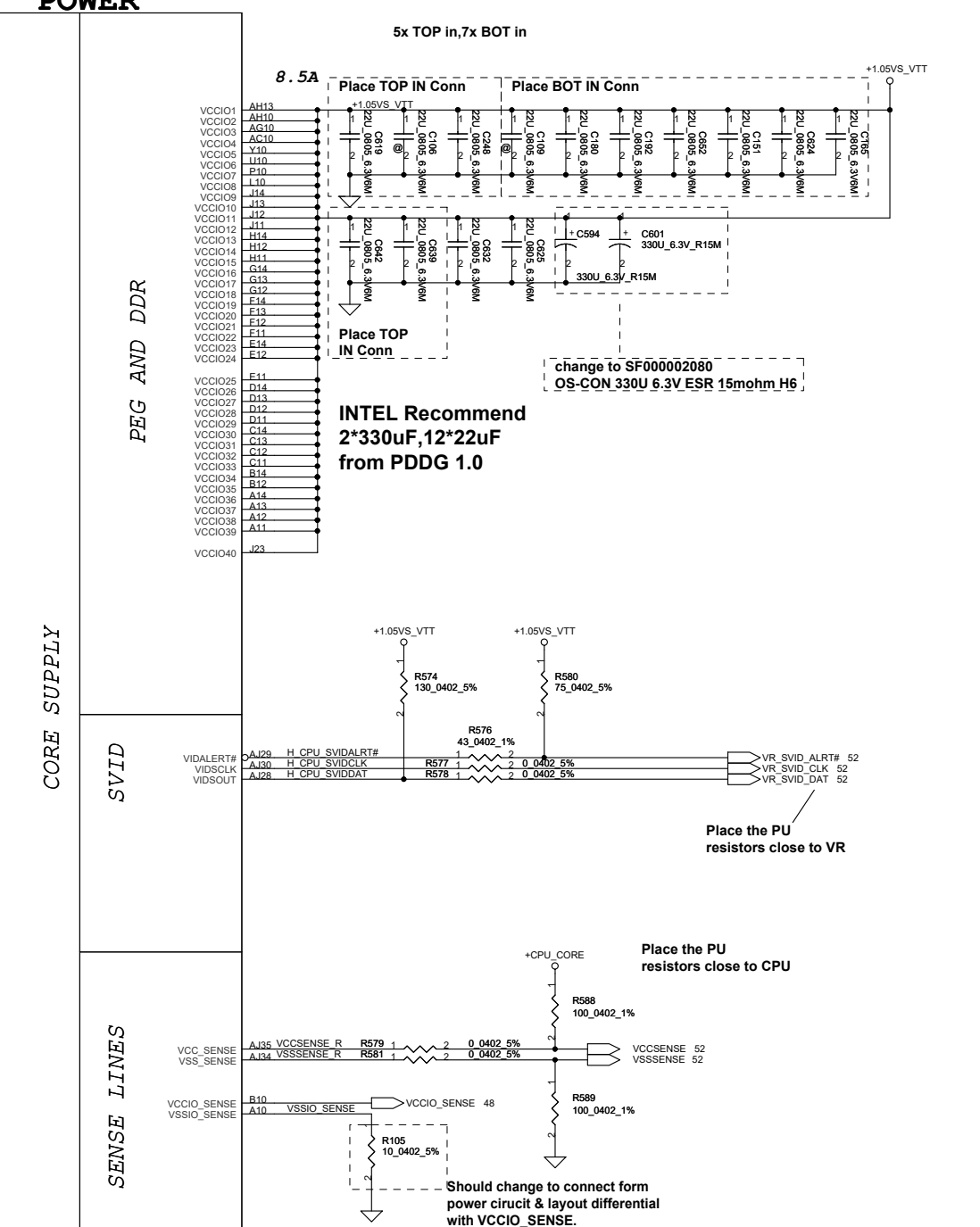
RESERVED

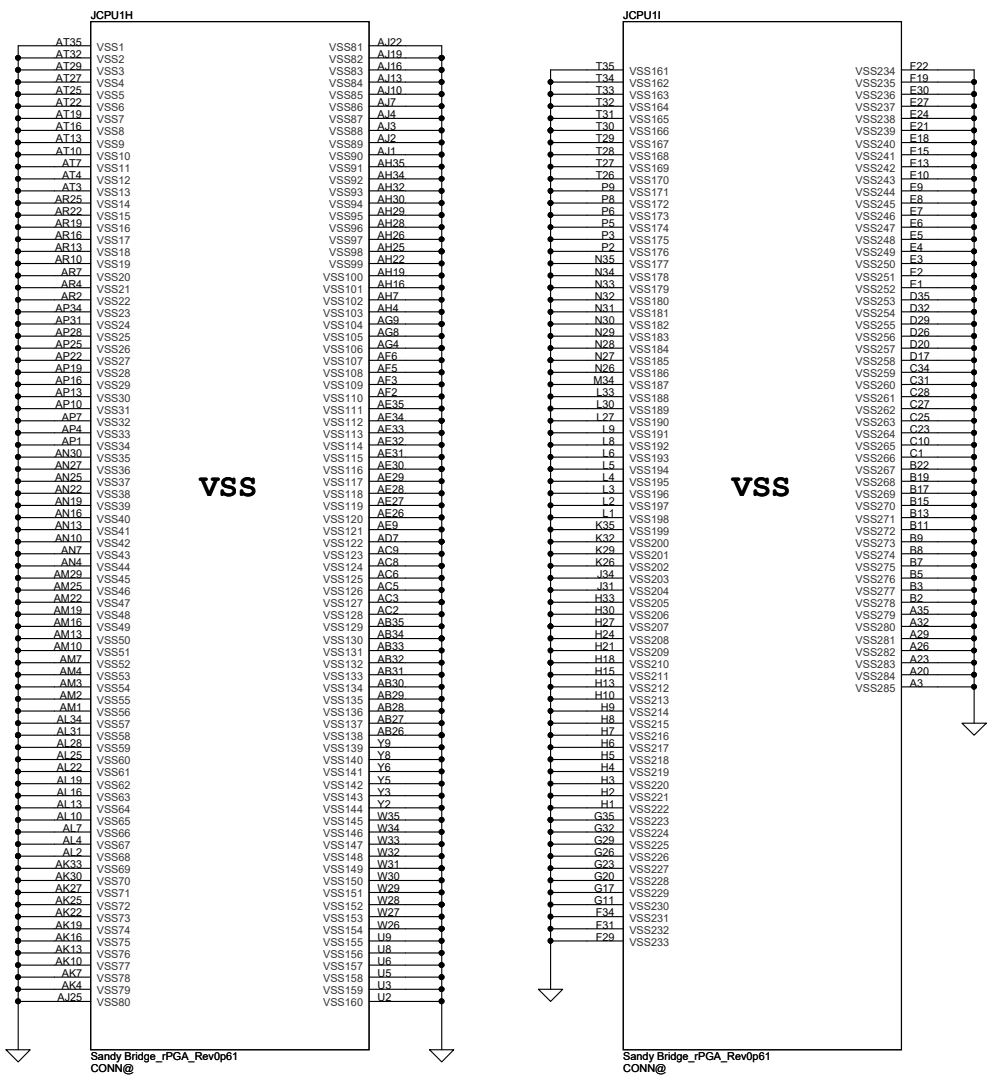
Sandy Bridge_rPGA_Rev0p61
 CONN@

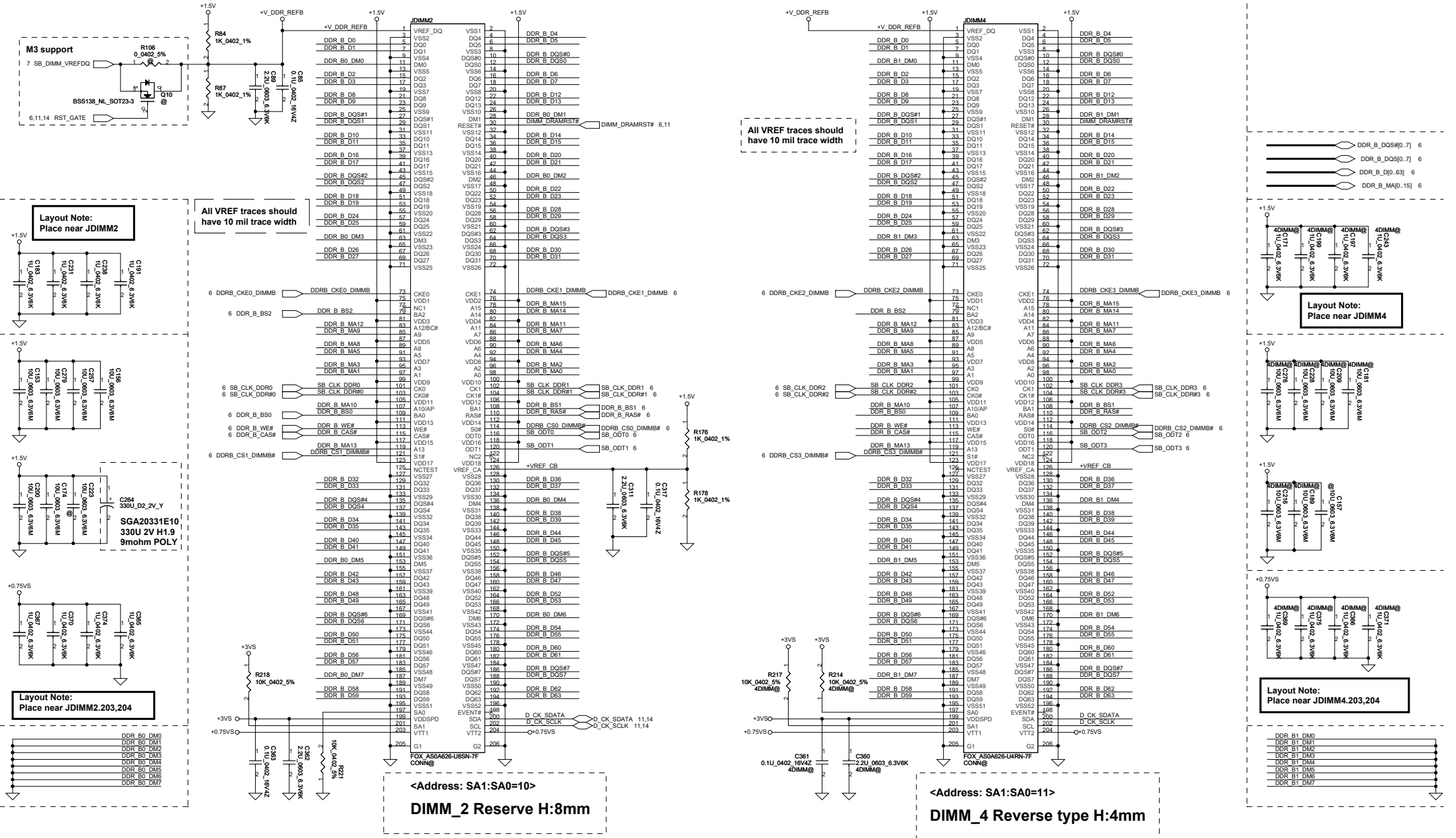
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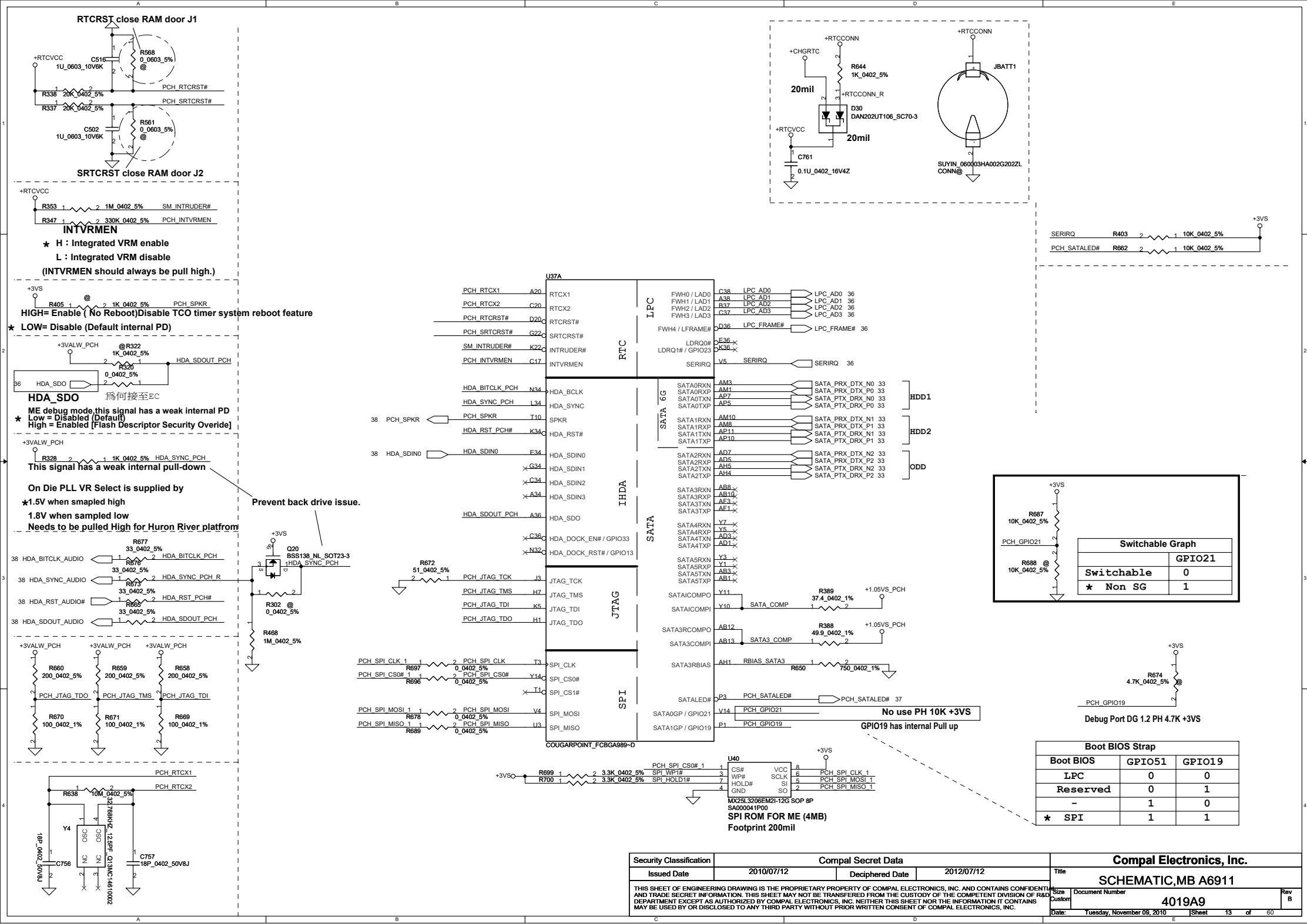


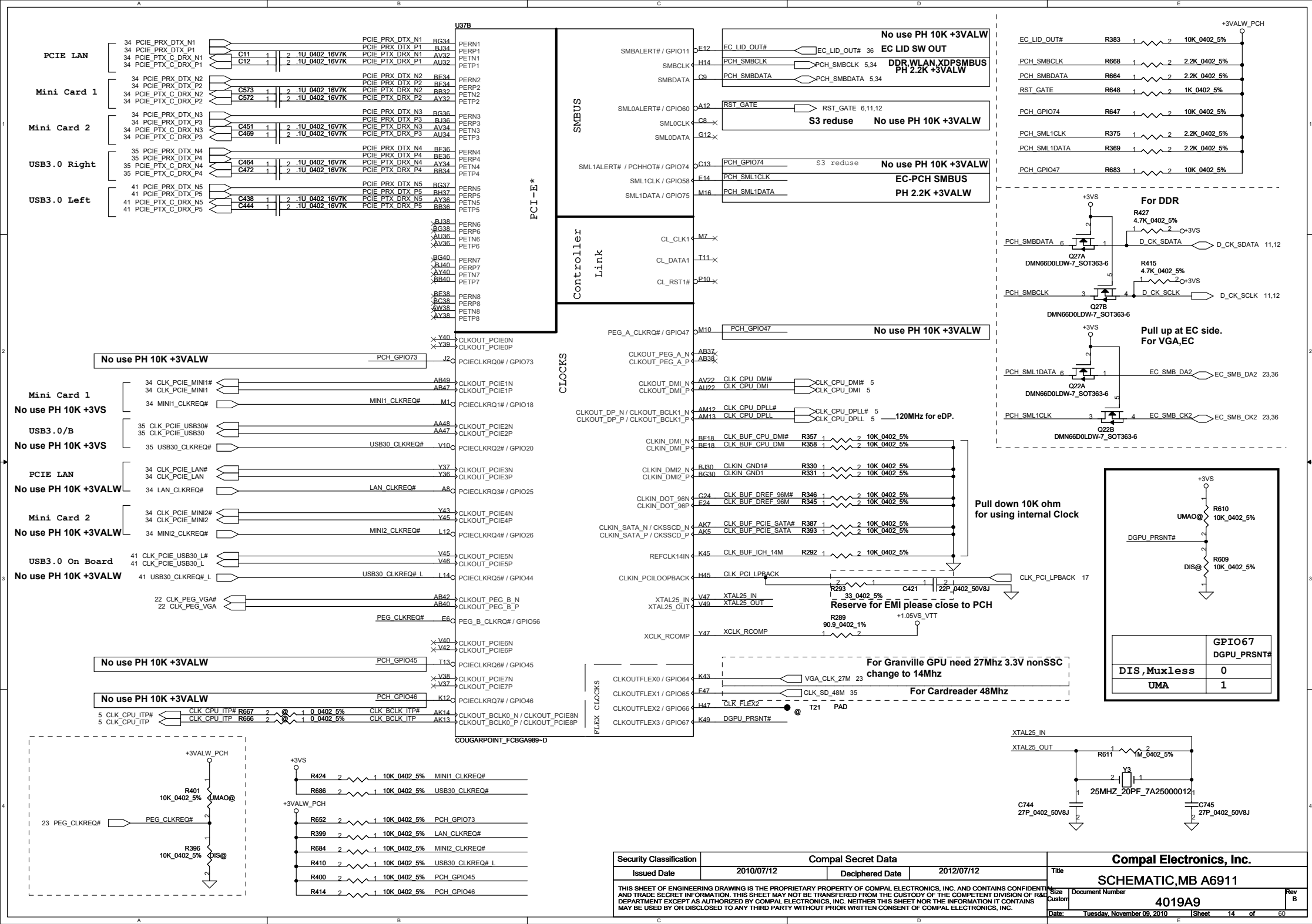
- POWER**
- PEG AND DDR**
- CORE SUPPLY**
- SVID**
- SENSE LINES**
- CONN@**

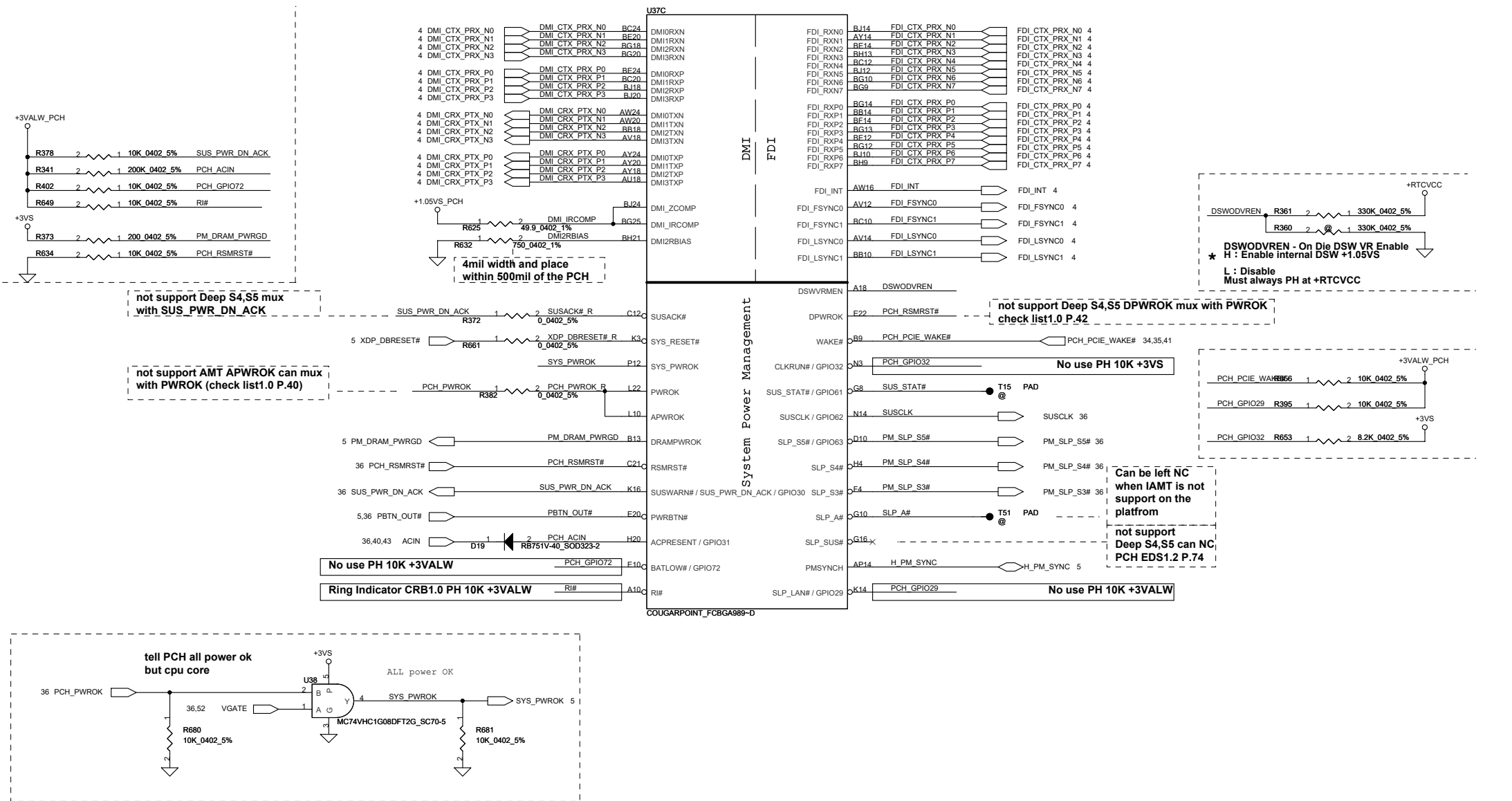


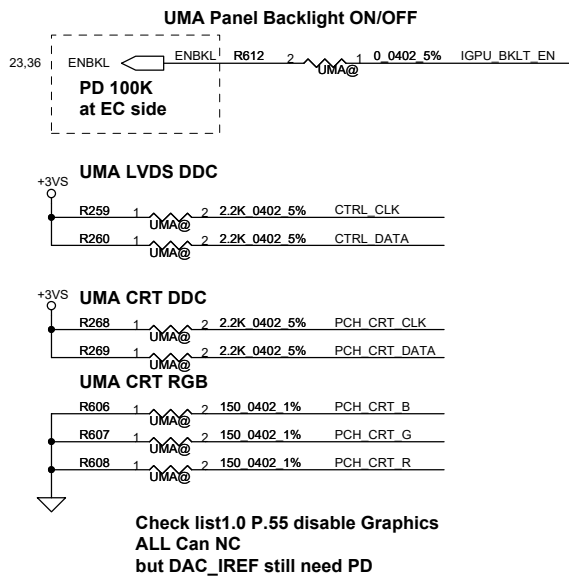








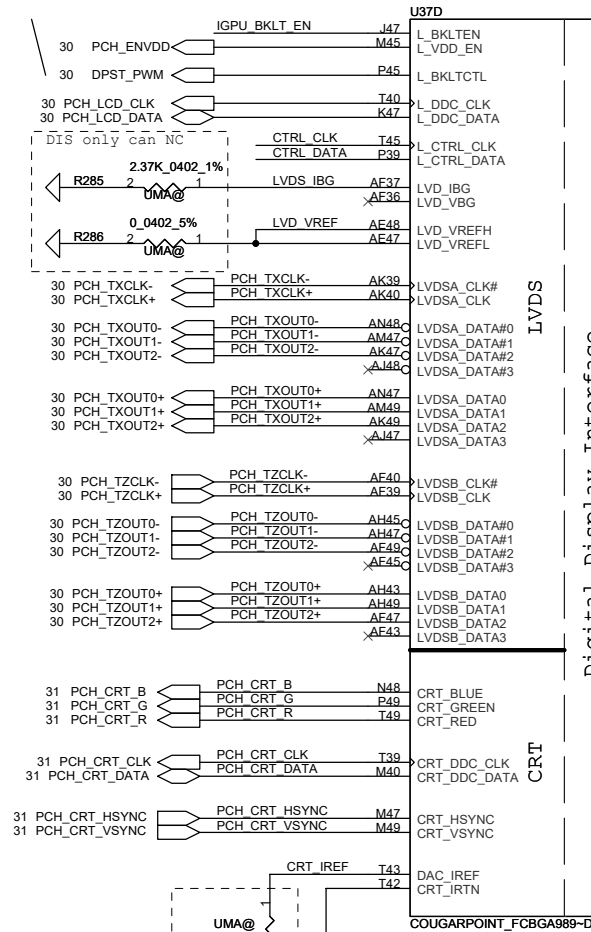




LVDS disable:
DATA/Clock/Control an NC
VCC_TX_LVDS,VCCA_LVDS PD to GND

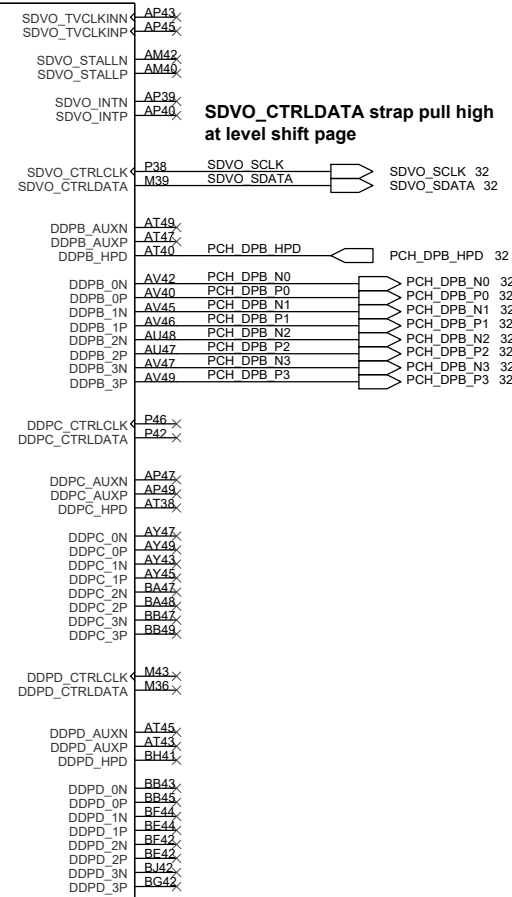
CRT disable:
DATA/Clock/Control an NC
VCCADAC connect to +3VS

Pull high at LVDS conn side.



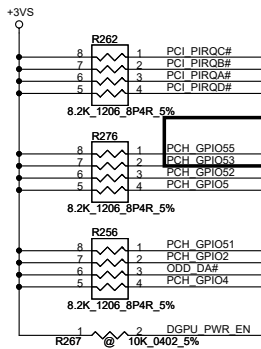
DIS only sku can use 1K_0402_5% to GND

Digital Display Interface



HDMI D2
HDMI D1
HDMI D0
HDMI CLK

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可以不用PH,如做GPIO使用PH+3VS

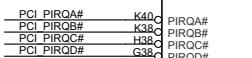
Boot BIOS Strap			
GPIO19 GPIO51 Boot BIOS			
GNT1#/ GPIO51	Bit11	Bit10	Destination
Internal	0	1	Reserved
PH	1	0	PCI
	1	1	SPI
	0	0	LPC

Only GPIO function

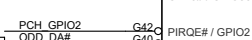
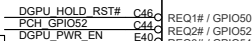
只剩GPIO的功能没有strap function
不做GPIO要PH+3VS,如做GPIO PH+3VS

只剩GPIO的功能没有strap function
無須PH(Internal PH),如做GPIO PH+3VS

PCI Interrupt Requests

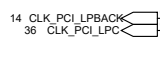


23,29,40,50,51 DGPU_PWR_EN



33 ODD_DA#

5.34,35,36,41 PLT_RST#

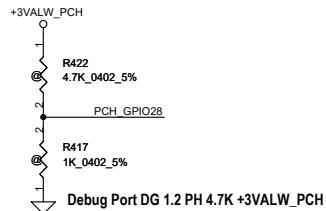


HDA_SYNC PH(PLL =+1.5VS)

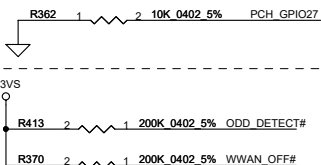
GPIO28

On-Die PLL Voltage Regulator

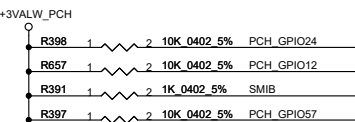
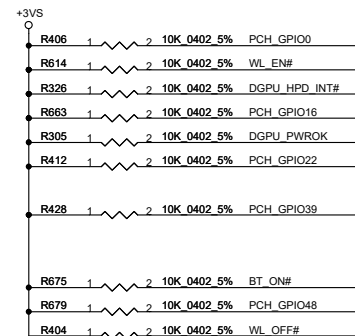
This signal has a weak internal pull up
* L : On-Die PLL voltage regulator enable
L : On-Die PLL Voltage Regulator disable



Deep S4,S5 wake event signal
RTC alarm,Power BTN,GPIO27
PCH_GPIO27 (Have internal Pull-High)
Deep S4,S5 wake event signal
No use PD to GND Check list1.0 P.70



SATA2GP/GPIO36 & SATA3GP/GPIO37
Sampled at Rising edge of PWROK.
Weak internal pull-down.
(weak internal pull-down is disabled
after PLTRST# de-asserts)
NOTE: This signal should NOT be
pulled high when strap is sampled



No use PH 10K +3VS
No use PH 10K +3VS
No use PH 10K +3VS

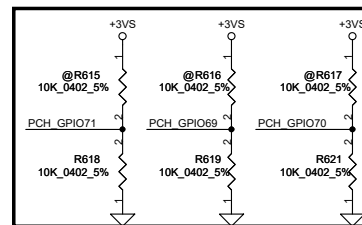
No use PH +3VALW
USB3.0 System management
Interrupt signal "SMI#".
No use PH +3VS

No use PH 10K +3VS
CRB1.0 PH 10K +3VALW
No use PD 10K to GND
No use PH 10K +3VALW
No use PH 10K +3VS BT ON/OFF
No use can NC
Can't PH
Can't PH
No use PH 10K +3VS Optimus(L)/ non optimus(H)
No use PH 10K +3VS
No use PH 10K +3VS
SATA5GP&TEMP_ALERT# CRB PH 10K +3VS
No use PH +3VALW or PD to GND

	GPIO38 OPTIMUS_EN#
* Muxless	0
nonMuxless	1

GPIO24 Unmultiplexed
NOTE: GPIO24 configuration
register bits are not cleared by
CF9h reset event.
CRB1.0 PH10K to +3VALW

Fan Tachometer Inputs
TACH1~7 only on server
can insted to GPIO



Project ID	GPIO69	GPIO70	GPIO71
* P7YE0	0	0	0
x	0	0	1
x	0	1	0
x	0	1	1
x	1	0	0
x	0	0	1
x	0	1	0
x	0	1	1
x	1	0	0
x	1	0	1
x	1	1	0
x	1	1	1

GPIO
CPU/MISC

NCTF

U37F

BMBUSY# / GPIO0
TACH1 / GPIO1
TACH2 / GPIO6
TACH3 / GPIO7
GPIO8
LAN_PHY_PWR_CTRL / GPIO12
GPIO15
SATA4GP / GPIO16
TACH0 / GPIO17
SCLOCK / GPIO22
GPIO24 / MEM_LED
GPIO27
GPIO28
STP_PCI# / GPIO34
GPIO35
SATA2GP / GPIO36
SATA3GP / GPIO37
SLOAD / GPIO38
SDATAOUT0 / GPIO39
SDATAOUT1 / GPIO48
SATA5GP / GPIO49
GPIO57

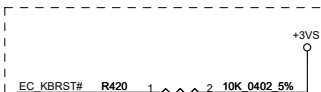
TACH4 / GPIO8
TACH5 / GPIO69
TACH6 / GPIO70
TACH7 / GPIO71

A20GATE
PECI
RCIN#
PROCWRGD
THRMTrip#
INIT3_3V#
NC_1
NC_2
NC_3
NC_4
NC_5

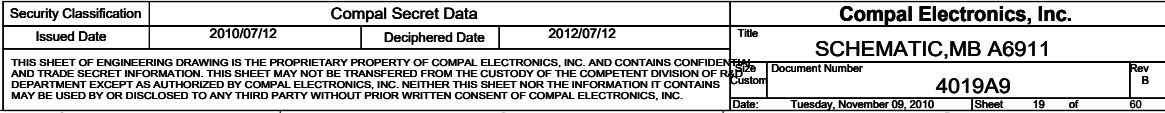
VSS_NCTF_15
VSS_NCTF_16
VSS_NCTF_17
VSS_NCTF_18
VSS_NCTF_19
VSS_NCTF_20
VSS_NCTF_21
VSS_NCTF_22
VSS_NCTF_23
VSS_NCTF_24
VSS_NCTF_25
VSS_NCTF_26
VSS_NCTF_27
VSS_NCTF_28
VSS_NCTF_29
VSS_NCTF_30
VSS_NCTF_31
VSS_NCTF_32

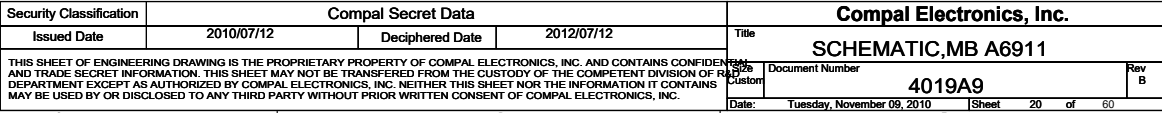
PECI CPU-EC
CTRL+ALT+DEL
non CPU power ok
130c shut sown

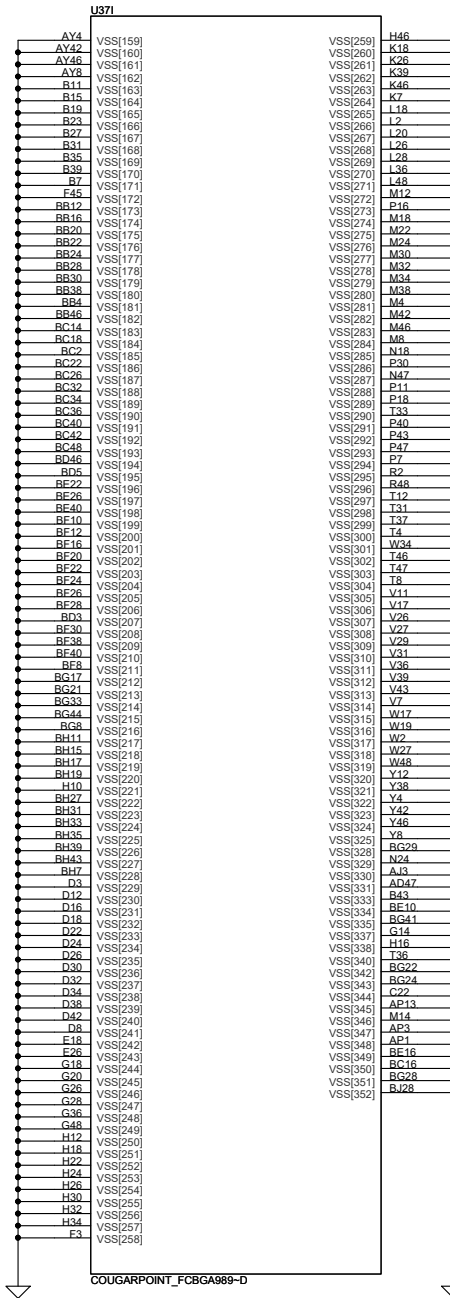
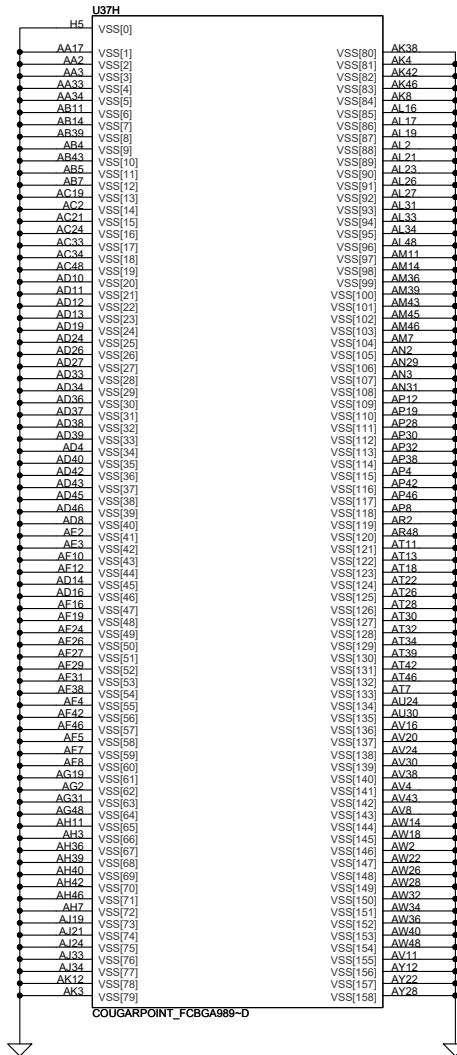
INIT3_3V
This signal has weak internal
PU, can't pull low,leave NC
TS_VSS1~4
PD to GND



COUGARPOINT_FCBGA989-D







4 PEG_GTX_HRX_N[0..15]
4 PEG_GTX_HRX_P[0..15]

4 PEG_HTX_C_GRX_N[0..15]
4 PEG_HTX_C_GRX_P[0..15]



U30G

LVDS CONTROL

VARY_BL
DIGON

AK27
A127

R133
10K_0402_5%

1
VGA@

2

R127
10K_0402_5%

1
VGA@

2

VGA_PNL_PWM 30
ENVDD 30

TXCLK_UP_DFP3P
TXCLK_UN_DFP3N

AK35
AL36

VGA_TZCLK+
VGA_TZCLK-

VGA_TZCLK+ 30
VGA_TZCLK- 30

TXOUT_U0P_DFP2P
TXOUT_U0N_DFP2N

AJ38
AK37

VGA_TZOUT0+
VGA_TZOUT0-

VGA_TZOUT0+ 30
VGA_TZOUT0- 30

TXOUT_U1P_DFP1P
TXOUT_U1N_DFP1N

AH35
AJ36

VGA_TZOUT1+
VGA_TZOUT1-

VGA_TZOUT1+ 30
VGA_TZOUT1- 30

TXOUT_U2P_DFP0P
TXOUT_U2N_DFP0N

AH37
AG38

VGA_TZOUT2+
VGA_TZOUT2-

VGA_TZOUT2+ 30
VGA_TZOUT2- 30

TXOUT_U3P
TXOUT_U3N

AF35
AG38

LVTMDP

TXCLK_LP_DPE3P
TXCLK_LN_DPE3N

AP34
AR34

VGA_TXCLK+
VGA_TXCLK-

VGA_TXCLK+ 30
VGA_TXCLK- 30

TXOUT_L0P_DPE2P
TXOUT_L0N_DPE2N

AW37
AU35

VGA_TXOUT0+
VGA_TXOUT0-

VGA_TXOUT0+ 30
VGA_TXOUT0- 30

TXOUT_L1P_DPE1P
TXOUT_L1N_DPE1N

AR37
AU39

VGA_TXOUT1+
VGA_TXOUT1-

VGA_TXOUT1+ 30
VGA_TXOUT1- 30

TXOUT_L2P_DPE0P
TXOUT_L2N_DPE0N

AP35
AR35

VGA_TXOUT2+
VGA_TXOUT2-

VGA_TXOUT2+ 30
VGA_TXOUT2- 30

TXOUT_L3P
TXOUT_L3N

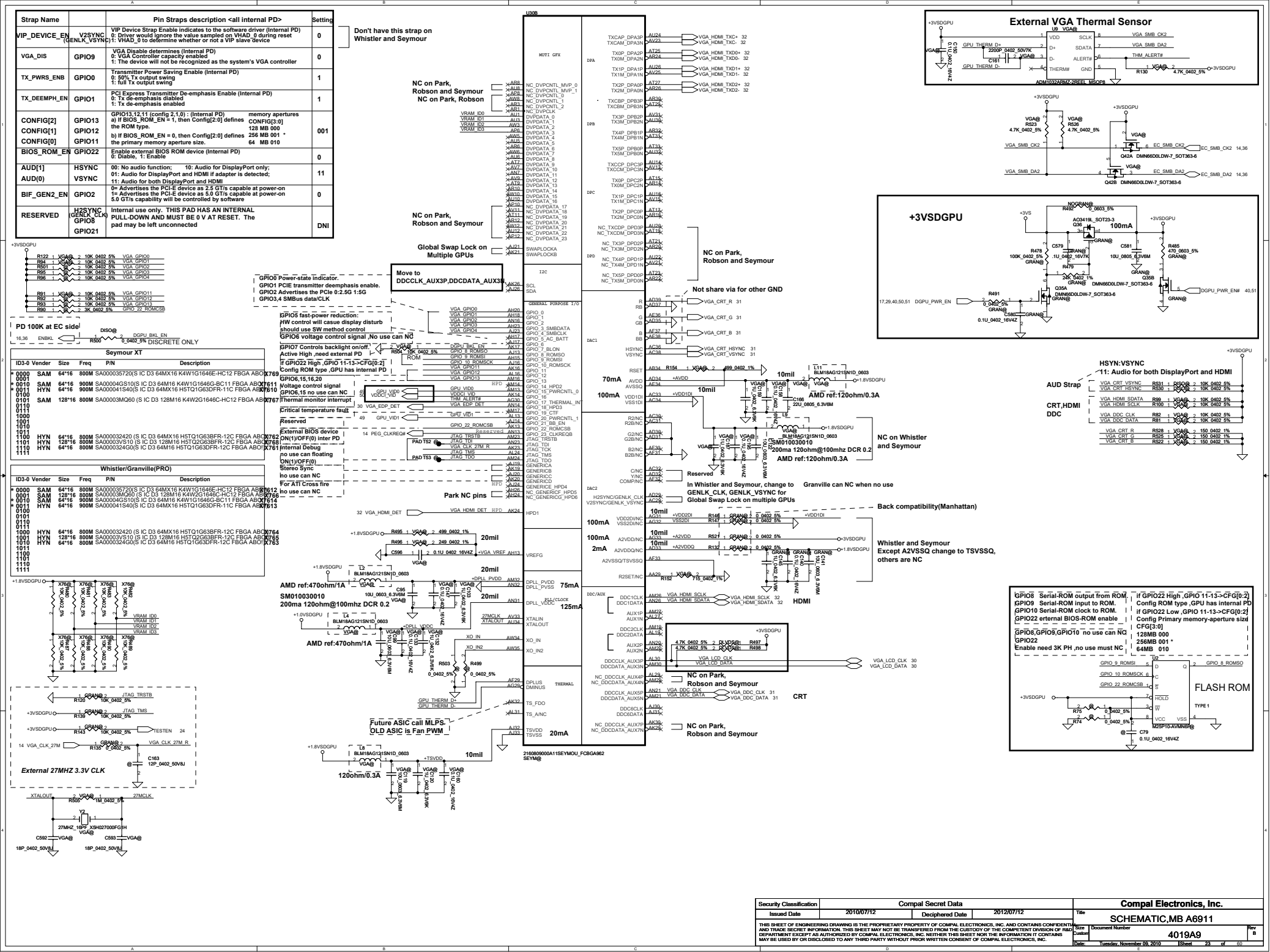
AN36
AP33

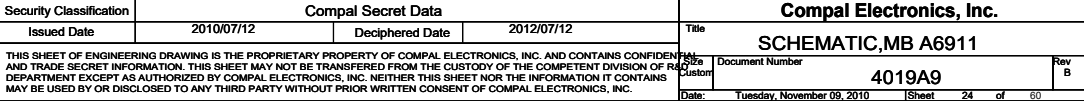
2180809000A11SEYMOU_FCBGA962

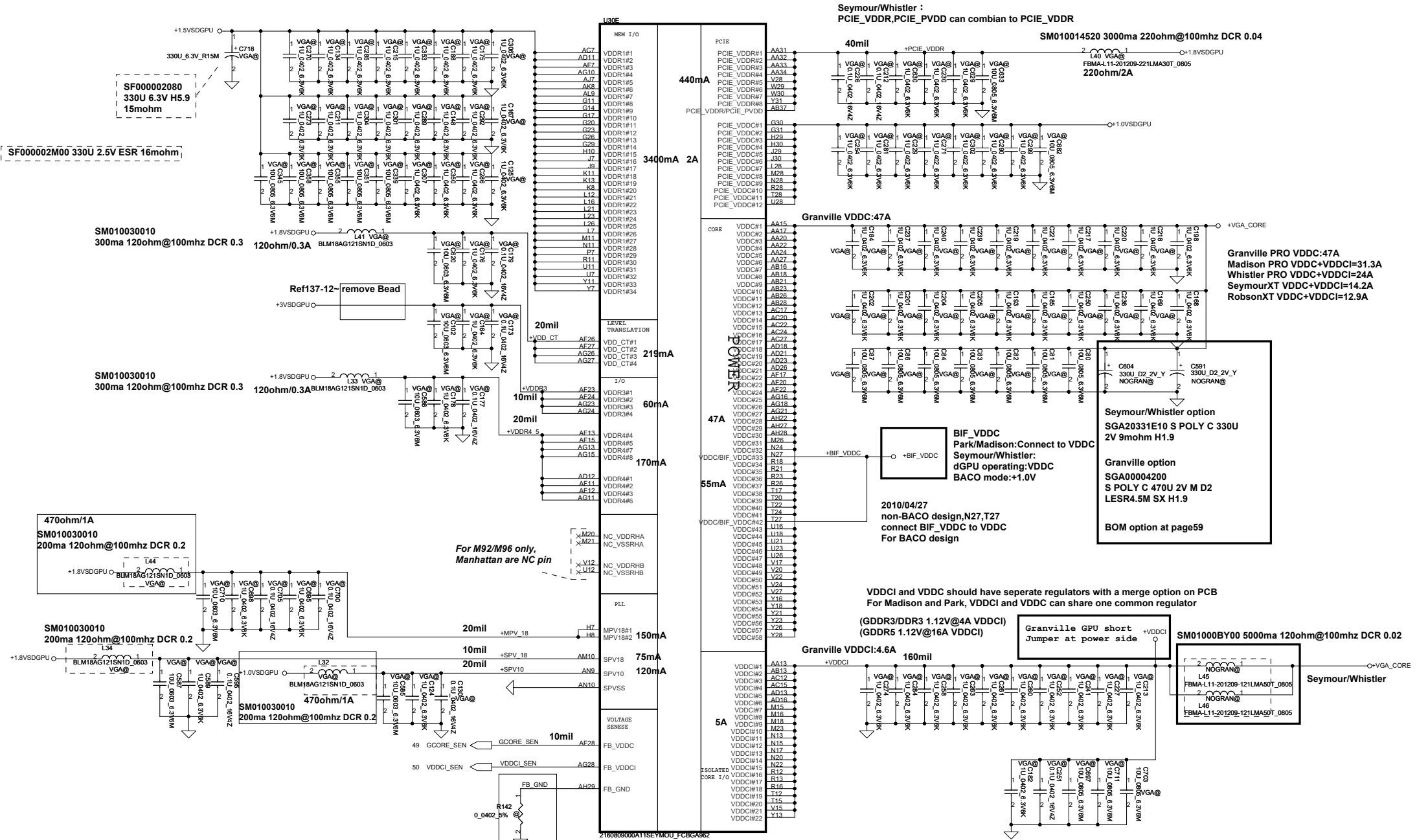
SEYM@

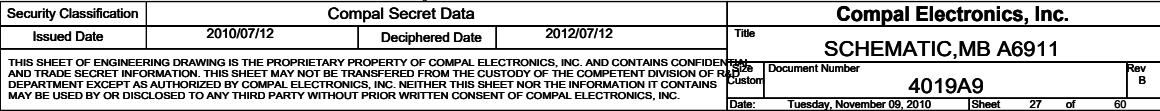
Display Port E config

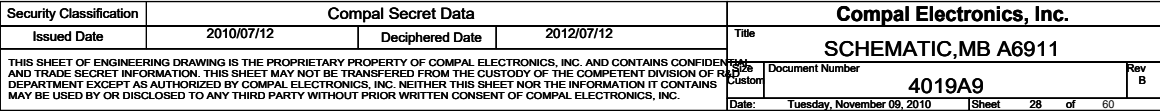
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Issued Date	2010/07/12	Deciphered Date	2012/07/12	Title
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			Size	Document Number
			A4	4019A9
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			Date:	Tuesday, November 09, 2010
			Sheet	22 of 60

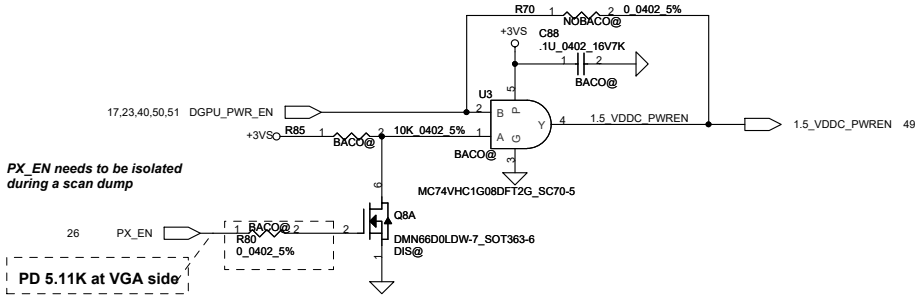






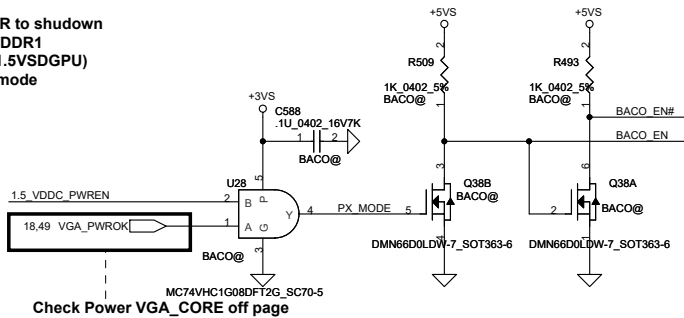




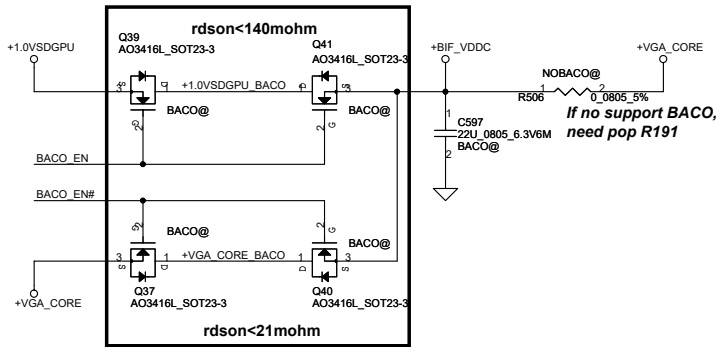


PX_EN = 1, For BACO Mode
PX_EN = 0, For Normal Mode

PX_EN:
Connect to PWR to shutdown
VDDC/VDDCI/VDDR1
(VGA_CORE, +1.5VSDGPU)
High in BACO mode



BACO_EN# = 1 (BACO mode)
BACO_EN# = 0 (Normal mode)
BACO_EN = 0 (BACO mode)
BACO_EN = 1 (Normal mode)



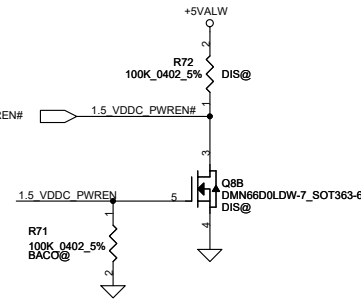
PX_EN = 1, For BACO Mode
BACO_EN = 0
BACO_EN# = 1(5V) ==> BIF_VDDC = +1.0VSDGPU
PX_EN = 0, For Normal Mode
BACO_EN = 1(5V) ==> BIF_VDDC = VGA_CORE
BACO_EN# = 0

For the MOSFETs on the path of delivering
PCIE_VDDC(+1.0VSDGPU) to
BIF_VDDC Rdson of 140 mOhms or less is required.

For the MOSFETs on the path of delivering VGA_CORE to
BIF_VDDC, Rdson of 21 mOhms or less is required.

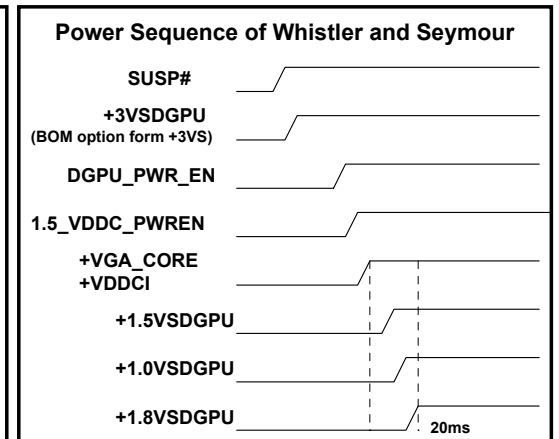
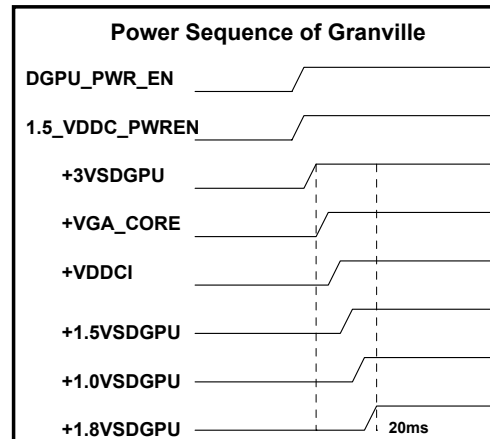
BACO_EN/BACO_EN#:
0: BACO Mode->BACO_EN High->
BIF_VDDC = +1.0VSDGPU(N-MOS), VGA_CORE(P-MOS)

1: Normal mode->BACO_EN# High->
BIF_VDDC = +VGA_CORE(N-MOS), VGA_CORE(N-MOS)



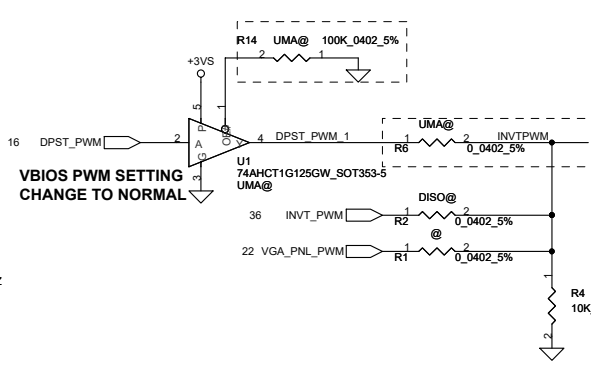
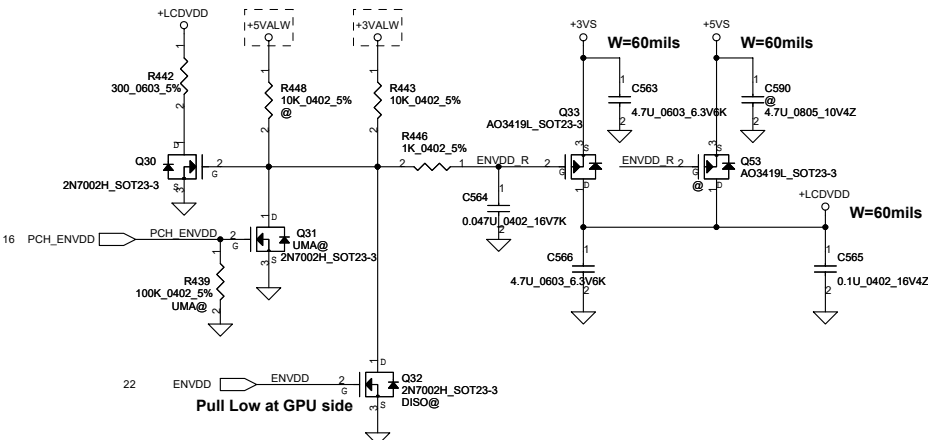
VGA Status Mapping table		
	Normal mode	BACO mode
PX_EN	0	1
1.5_VDDC_PWREN	1	0
BACO_EN#	1	0
BACO_EN	0	1
+3VSDGPU	ON	ON
+1.8VSDGPU	ON	ON
+1.0VSDGPU	ON	ON
+VGA_CORE	ON	OFF
+1.5VSDGPU	ON	OFF
+BIF_VDDC	+VGA_CORE	+1.0VSDGPU

VGA Power Enable Signal Mapping table		
	Graville	Whistler and Seymour
+3VSDGPU	DGPU_PWR_EN	SUSP#
+1.8VSDGPU	DGPU_PWR_EN	DGPU_PWR_EN
+1.0VSDGPU	DGPU_PWR_EN	DGPU_PWR_EN
+VDDCI	DGPU_PWR_EN	Combine with +VGA_CORE
+VGA_CORE	DGPU_PWR_EN	1.5_VDDC_PWREN
+1.5VSDGPU	DGPU_PWR_EN	1.5_VDDC_PWREN



100505 change to +3VALW
101029 add +5VALW

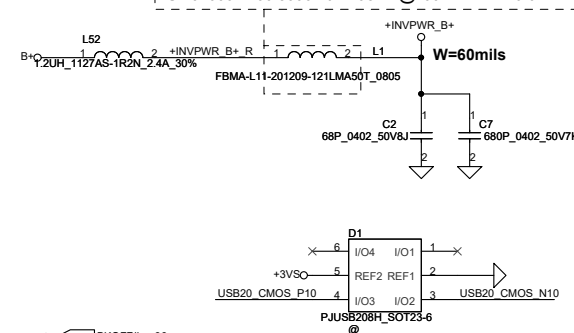
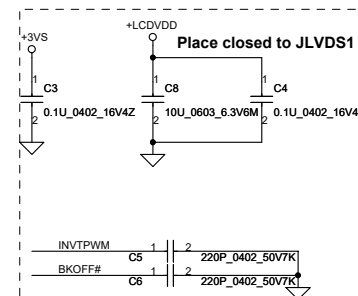
LCD POWER CIRCUIT



UMA/DIS LVDS/eDP Mapping table				
UMA	DIS			Panel Conn.
LVDS	eDP	LVDS	eDP	
PCH_TXOUT0+		VGA_TXOUT0+		TXOUT0+
PCH_TXOUT0-		VGA_TXOUT0-		TXOUT0-
PCH_TXOUT1+	EDP_TXP1	VGA_TXOUT1+	DP1P	TXOUT1+
PCH_TXOUT1-	EDP_TXN1	VGA_TXOUT1-	DP1N	TXOUT1-
PCH_TXOUT2+	EDP_TXP0	VGA_TXOUT2+	DP0P	TXOUT2+
PCH_TXOUT2-	EDP_TXN0	VGA_TXOUT2-	DP0N	TXOUT2-
PCH_TXCLK+		VGA_TXCLK+		TXCLK+
PCH_TXCLK-		VGA_TXCLK-		TXCLK-
PCH_TZOUT0+		VGA_TZOUT0+		TZOUT0+
PCH_TZOUT0-		VGA_TZOUT0-		TZOUT0-
PCH_TZOUT1+		VGA_TZOUT1+		TZOUT1+
PCH_TZOUT1-		VGA_TZOUT1-		TZOUT1-
PCH_TZOUT2+		VGA_TZOUT2+		TZOUT2+
PCH_TZOUT2-		VGA_TZOUT2-		TZOUT2-
PCH_TZCLK+		VGA_TZCLK+		TZCLK+
PCH_TZCLK-		VGA_TZCLK-		TZCLK-
PCH_I2CC_CLK	EDP_AUXP	VGA_LCD_CLK	AUXP	I2CC_SCL
PCH_I2CC_DATA	EDP_AUXN	VGA_LCD_DATA	AUXN	I2CC_SDA

SM010014520 3000ma 220ohm@100mhz DCR 0.04

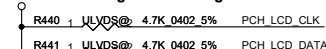
SM01000BY00 5000ma 120ohm@100mhz DCR 0.02



UMA ONLY/Muxless

16 PCH_TXOUT0+	PCH_TXOUT0+	R452	1	LVDS@	0.0402 5%	TXOUT0+
16 PCH_TXOUT0-	PCH_TXOUT0-	R450	1	LVDS@	0.0402 5%	TXOUT0-
16 PCH_TXOUT1+	PCH_TXOUT1+	R455	1	LVDS@	0.0402 5%	TXOUT1+
16 PCH_TXOUT1-	PCH_TXOUT1-	R453	1	LVDS@	0.0402 5%	TXOUT1-
16 PCH_TXOUT2+	PCH_TXOUT2+	R456	1	LVDS@	0.0402 5%	TXOUT2+
16 PCH_TXOUT2-	PCH_TXOUT2-	R454	1	LVDS@	0.0402 5%	TXOUT2-
16 PCH_TXCLK+	PCH_TXCLK+	R458	1	LVDS@	0.0402 5%	TXCLK+
16 PCH_TXCLK-	PCH_TXCLK-	R457	1	LVDS@	0.0402 5%	TXCLK-
16 PCH_TZOUT0+	PCH_TZOUT0+	R460	1	LVDS@	0.0402 5%	TZOUT0+
16 PCH_TZOUT0-	PCH_TZOUT0-	R459	1	LVDS@	0.0402 5%	TZOUT0-
16 PCH_TZOUT1+	PCH_TZOUT1+	R462	1	LVDS@	0.0402 5%	TZOUT1+
16 PCH_TZOUT1-	PCH_TZOUT1-	R461	1	LVDS@	0.0402 5%	TZOUT1-
16 PCH_TZOUT2+	PCH_TZOUT2+	R465	1	LVDS@	0.0402 5%	TZOUT2+
16 PCH_TZOUT2-	PCH_TZOUT2-	R463	1	LVDS@	0.0402 5%	TZOUT2-
16 PCH_TZCLK+	PCH_TZCLK+	R467	1	LVDS@	0.0402 5%	TZCLK+
16 PCH_TZCLK-	PCH_TZCLK-	R466	1	LVDS@	0.0402 5%	TZCLK-
16 PCH_LCD_CLK	PCH_LCD_CLK	R444	1	LVDS@	0.0402 5%	I2CC_SCL
16 PCH_LCD_DATA	PCH_LCD_DATA	R445	1	LVDS@	0.0402 5%	I2CC_SDA

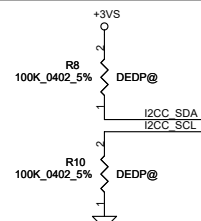
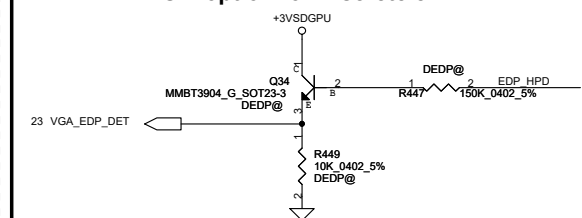
5/4 PCH_LCD_CLK & PCH_LCD_DATA
Pull high 2.2K change to 4.7K



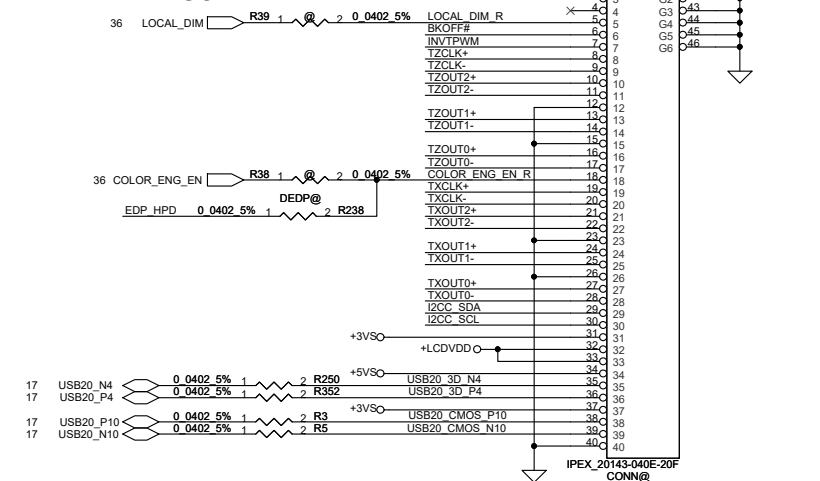
Discrete ONLY

22 VGA_TXOUT0+	VGA_TXOUT0+	R13	1	LVDS@	0.0402 5%	TXOUT0+
22 VGA_TXOUT0-	VGA_TXOUT0-	R12	1	LVDS@	0.0402 5%	TXOUT0-
22 VGA_TXOUT1+	VGA_TXOUT1+	R13	1	LVDS@	0.0402 5%	TXOUT1+
22 VGA_TXOUT1-	VGA_TXOUT1-	R17	1	LVDS@	0.0402 5%	TXOUT1-
22 VGA_TXOUT2+	VGA_TXOUT2+	R24	1	LVDS@	0.0402 5%	TXOUT2+
22 VGA_TXOUT2-	VGA_TXOUT2-	R22	1	LVDS@	0.0402 5%	TXOUT2-
22 VGA_TXCLK+	VGA_TXCLK+	R26	1	LVDS@	0.0402 5%	TXCLK+
22 VGA_TXCLK-	VGA_TXCLK-	R25	1	LVDS@	0.0402 5%	TXCLK-
22 VGA_TZOUT0+	VGA_TZOUT0+	R28	1	LVDS@	0.0402 5%	TZOUT0+
22 VGA_TZOUT0-	VGA_TZOUT0-	R27	1	LVDS@	0.0402 5%	TZOUT0-
22 VGA_TZOUT1+	VGA_TZOUT1+	R30	1	LVDS@	0.0402 5%	TZOUT1+
22 VGA_TZOUT1-	VGA_TZOUT1-	R29	1	LVDS@	0.0402 5%	TZOUT1-
22 VGA_TZOUT2+	VGA_TZOUT2+	R32	1	LVDS@	0.0402 5%	TZOUT2+
22 VGA_TZOUT2-	VGA_TZOUT2-	R31	1	LVDS@	0.0402 5%	TZOUT2-
22 VGA_TZCLK+	VGA_TZCLK+	R34	1	LVDS@	0.0402 5%	TZCLK+
22 VGA_TZCLK-	VGA_TZCLK-	R33	1	LVDS@	0.0402 5%	TZCLK-
AUX_P VGA_LCD_CLK	VGA_LCD_CLK	R9	1	LVDS@	0.0402 5%	I2CC_SCL
AUX_P VGA_LCD_DATA	VGA_LCD_DATA	R7	1	LVDS@	0.0402 5%	I2CC_SDA

BOM option for Discrete eDP



LED PANEL Conn.



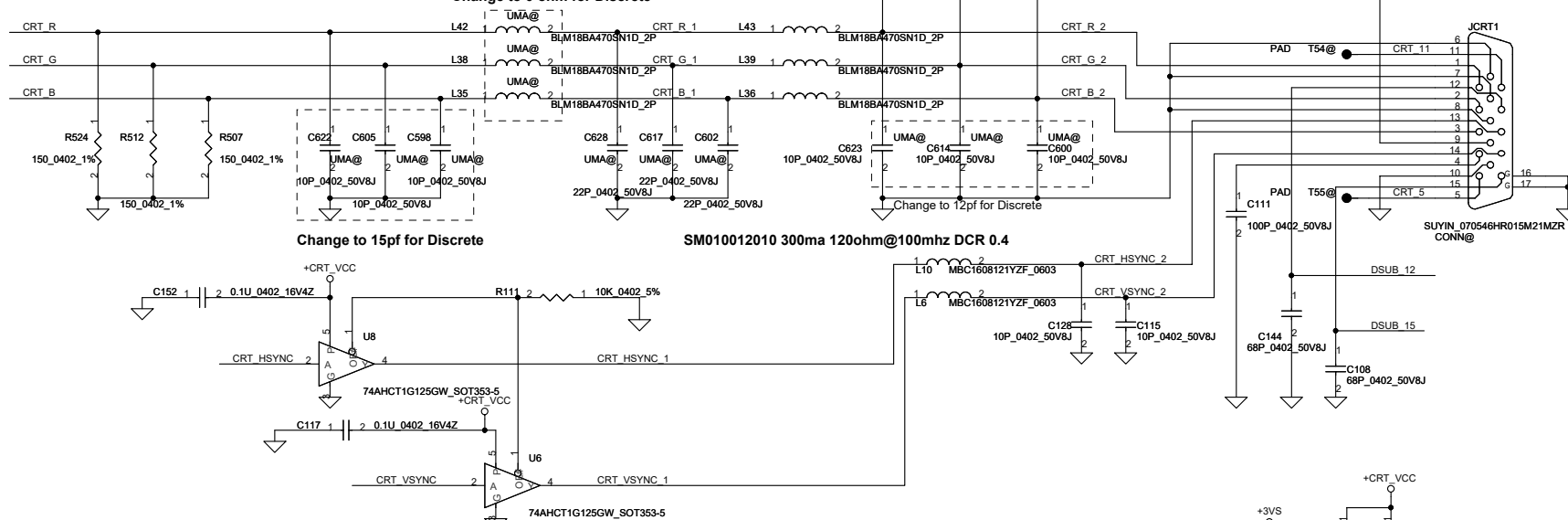
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Customer					4019A9
Date:	Tuesday, November 09, 2010	Sheet	30	of	60

CRT Connector

CRB1.0 use 47ohm@100Mhz Bead

SM01000GA00 300mA 47ohm@100Mhz DCR 0.55

Change to 0 ohm for Discrete



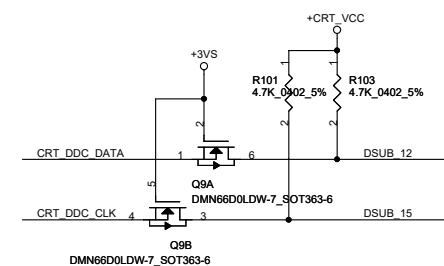
UMA only/Muxless

16	PCH_CRT_R	PCH_CRT_R	R529	2	UMA@	1	0.0402	5%	CRT_R
16	PCH_CRT_G	PCH_CRT_G	R519	2	UMA@	1	0.0402	5%	CRT_G
16	PCH_CRT_B	PCH_CRT_B	R511	2	UMA@	1	0.0402	5%	CRT_B
16	PCH_CRT_HSYNC	PCH_CRT_HSYNC	R137	2	UMA@	1	33.0402	5%	CRT_HSYNC
16	PCH_CRT_VSYNC	PCH_CRT_VSYNC	R110	2	UMA@	1	33.0402	5%	CRT_VSYNC
16	PCH_CRT_CLK	PCH_CRT_CLK	R102	2	UMA@	1	0.0402	5%	CRT_DDC_CLK
16	PCH_CRT_DATA	PCH_CRT_DATA	R89	2	UMA@	1	0.0402	5%	CRT_DDC_DATA

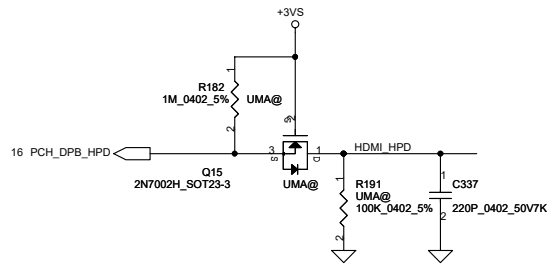
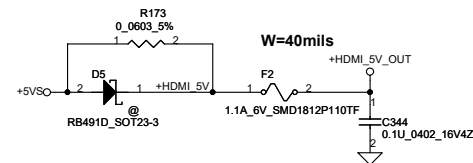
PCH DDC PU 2.2K on Page 17

Discrete only

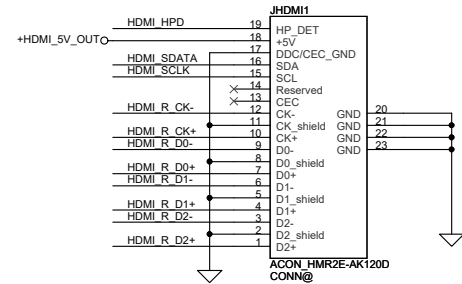
23	VGA_CRT_R	VGA CRT R	R527	2	RISOR	1	0.0402	5%	CRT R
23	VGA_CRT_G	VGA CRT G	R514	2	RISOR	1	0.0402	5%	CRT G
23	VGA_CRT_B	VGA CRT B	R510	2	RISOR	1	0.0402	5%	CRT B
23	VGA_CRT_HSYNC	VGA CRT HSYNC	R131	2	RISOR	1	0.0402	5%	CRT HSYNC
23	VGA_CRT_VSYNC	VGA CRT VSYNC	R107	2	RISOR	1	0.0402	5%	CRT VSYNC
23	VGA_DDC_CLK	VGA DDC CLK	R98	2	RISOR	1	0.0402	5%	CRT DDC CLK
23	VGA_DDC_DATA	VGA DDC DATA	R86	2	RISOR	1	0.0402	5%	CRT DDC DATA



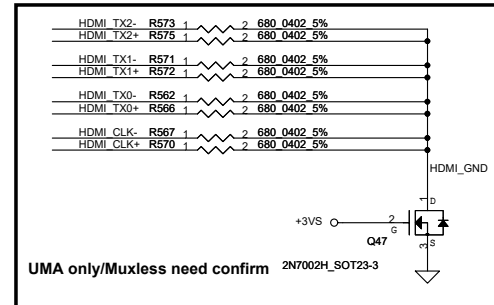
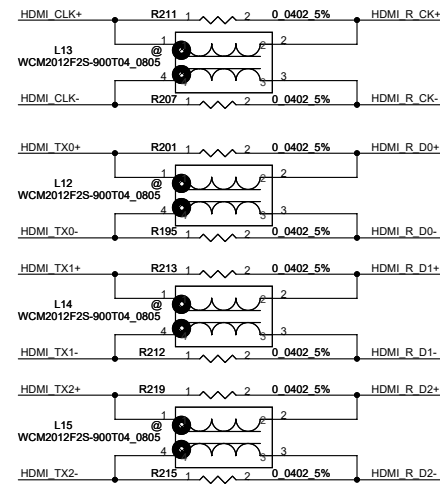
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				Date:	Tuesday, November 09, 2010	Sheet 31 of 60



HDMI connector

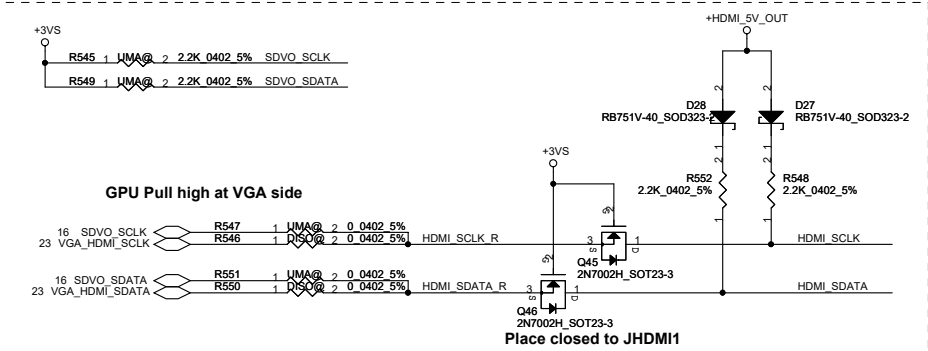
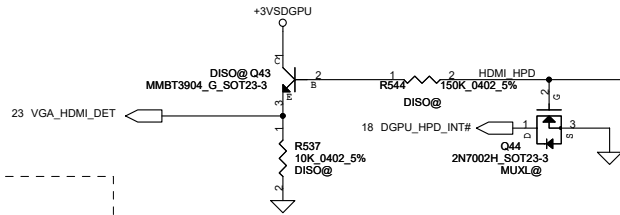


SM070001310 400ma 90ohm@100mhz DCR 0.3



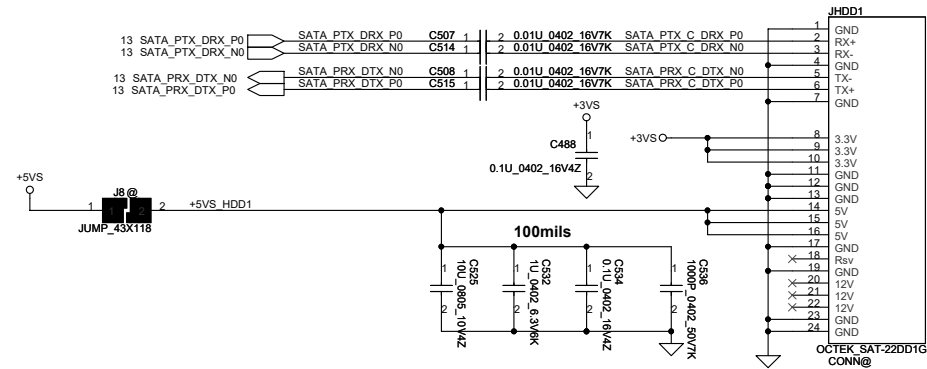
UMA/Muxless			
16 PCH_DPB_N0	C364 UMA@ 2	1 .1U 0402 16V7K	HDMI TX2-
16 PCH_DPB_P0	C368 UMA@ 2	1 .1U 0402 16V7K	HDMI TX2+
16 PCH_DPB_N1	C357 UMA@ 2	1 .1U 0402 16V7K	HDMI TX1-
16 PCH_DPB_P1	C359 UMA@ 2	1 .1U 0402 16V7K	HDMI TX1+
16 PCH_DPB_N2	C347 UMA@ 2	1 .1U 0402 16V7K	HDMI TX0-
16 PCH_DPB_P2	C349 UMA@ 2	1 .1U 0402 16V7K	HDMI TX0+
16 PCH_DPB_N3	C352 UMA@ 2	1 .1U 0402 16V7K	HDMI CLK-
16 PCH_DPB_P3	C356 UMA@ 2	1 .1U 0402 16V7K	HDMI CLK+

DIS Only			
23 VGA_HDMI_TXD2-	C716 DISO@ 2	1 .1U 0402 16V7K	HDMI TX2-
23 VGA_HDMI_TXD2+	C717 DISO@ 2	1 .1U 0402 16V7K	HDMI TX2+
23 VGA_HDMI_TXD1-	C714 DISO@ 2	1 .1U 0402 16V7K	HDMI TX1-
23 VGA_HDMI_TXD1+	C715 DISO@ 2	1 .1U 0402 16V7K	HDMI TX1+
23 VGA_HDMI_TXD0-	C704 DISO@ 2	1 .1U 0402 16V7K	HDMI TX0-
23 VGA_HDMI_TXD0+	C709 DISO@ 2	1 .1U 0402 16V7K	HDMI TX0+
23 VGA_HDMI_TXC-	C712 DISO@ 2	1 .1U 0402 16V7K	HDMI CLK-
23 VGA_HDMI_TXC+	C713 DISO@ 2	1 .1U 0402 16V7K	HDMI CLK+



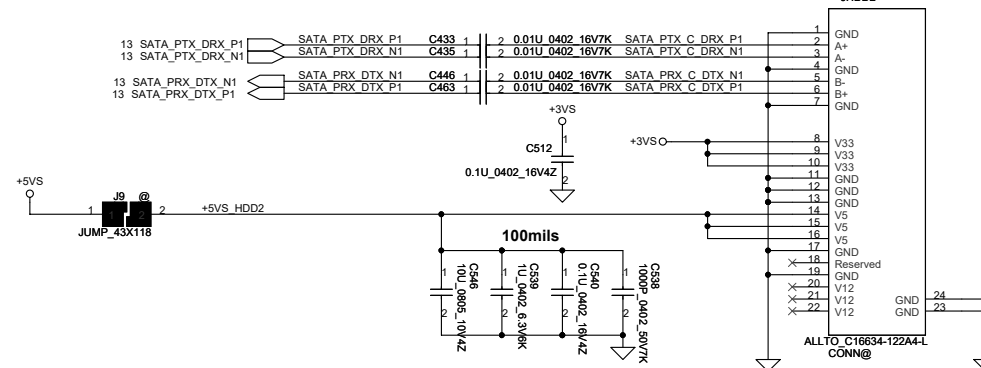
SATA HDD1 Conn.

CL 2.9 mm



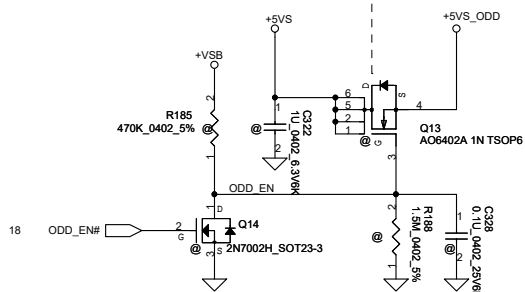
SATA HDD2 Conn.

CL 4.4 mm



SATA ODD Conn.

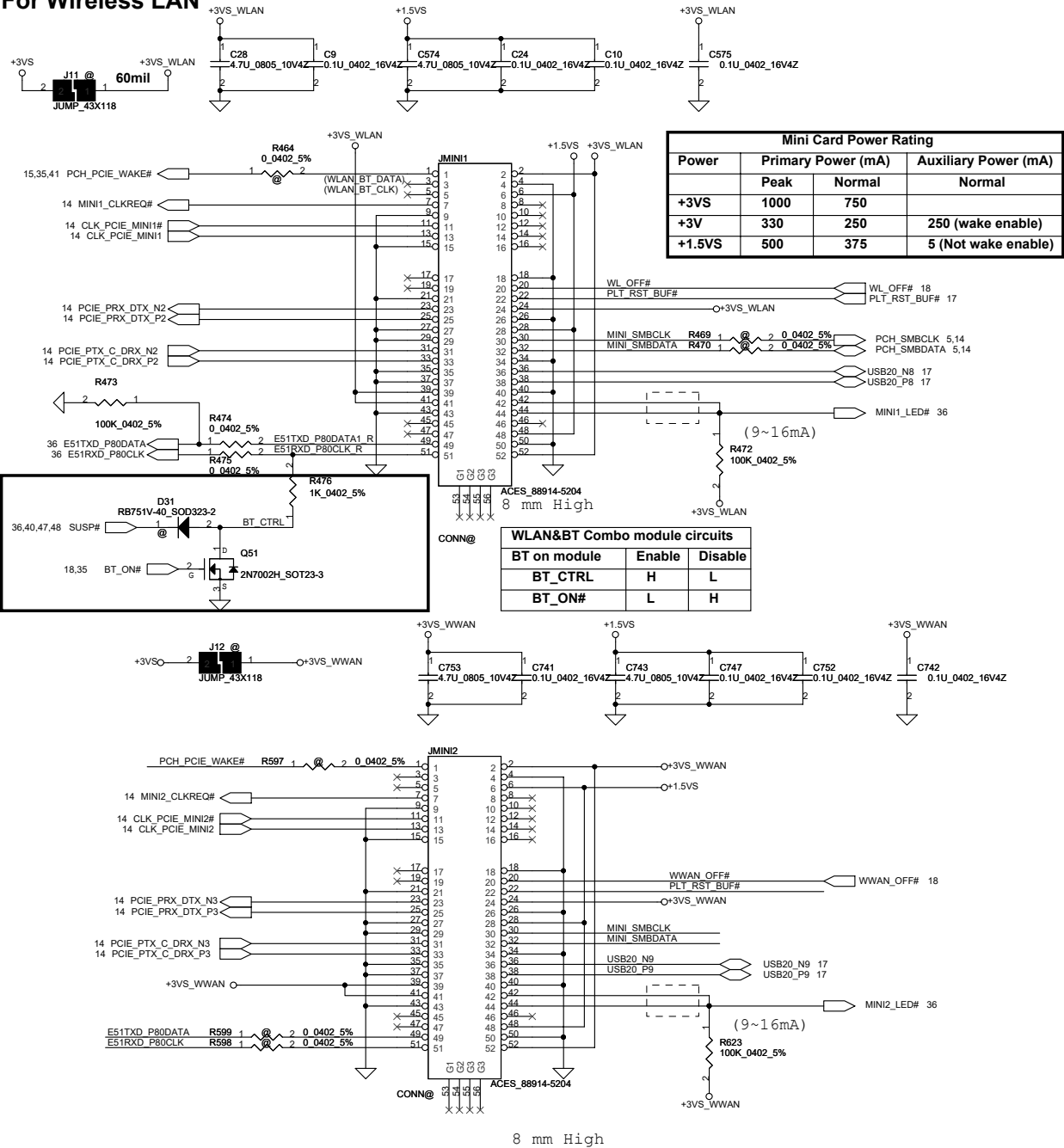
SB564020020(S TR A06402A 1N TSOP-6 W/D)



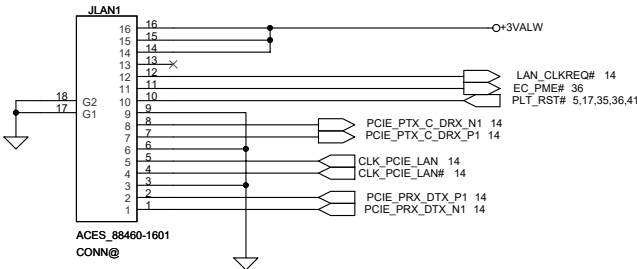
Place Cap near ODD Conn.

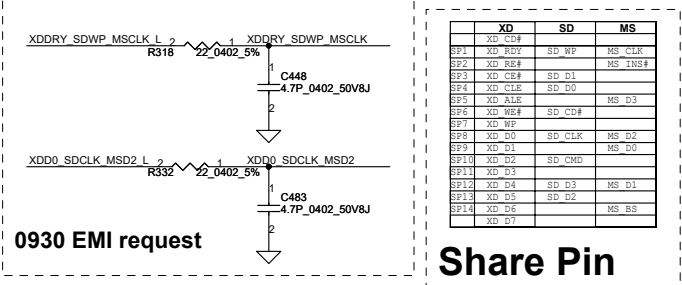
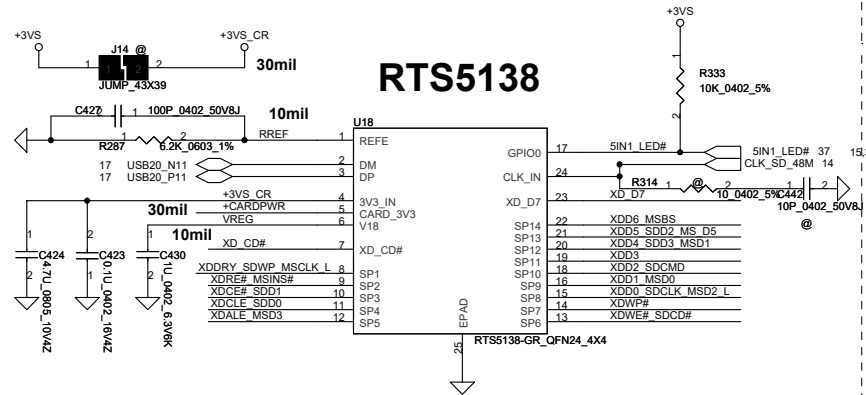
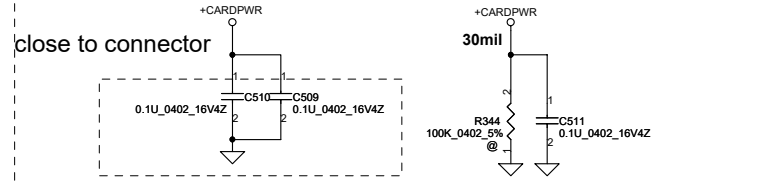
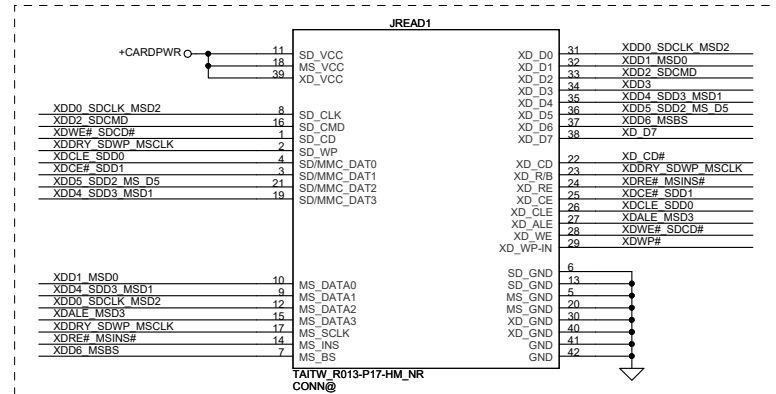
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For Wireless LAN

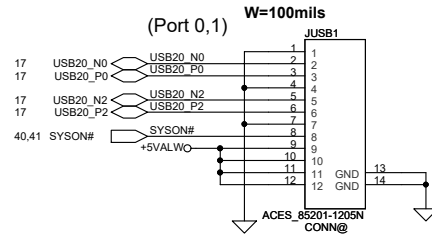


LAN CONN. LS-6912P



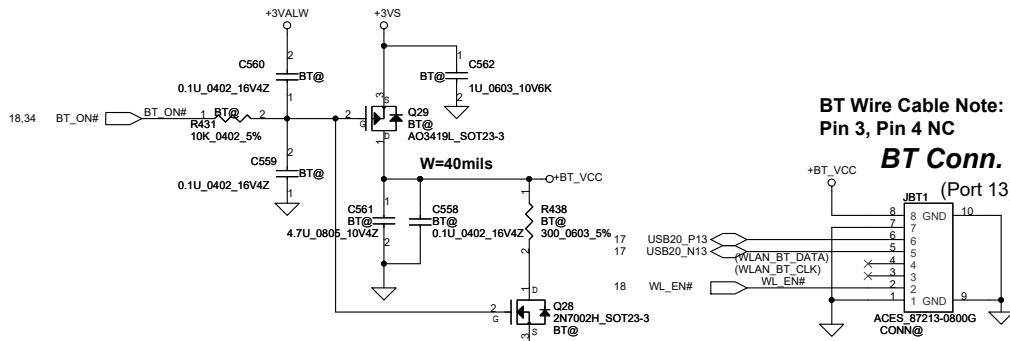
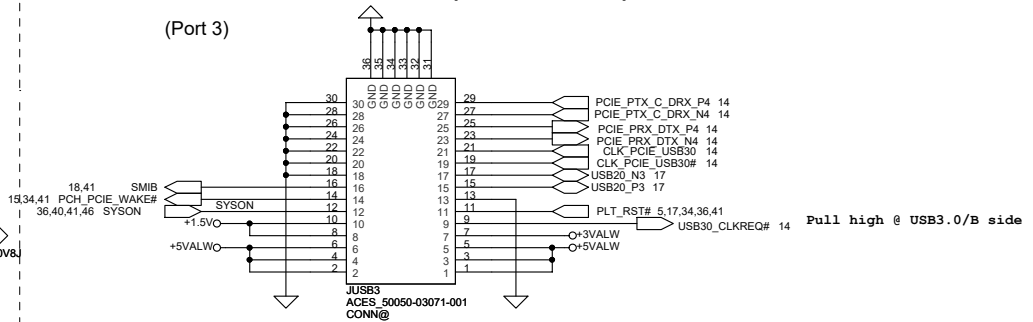


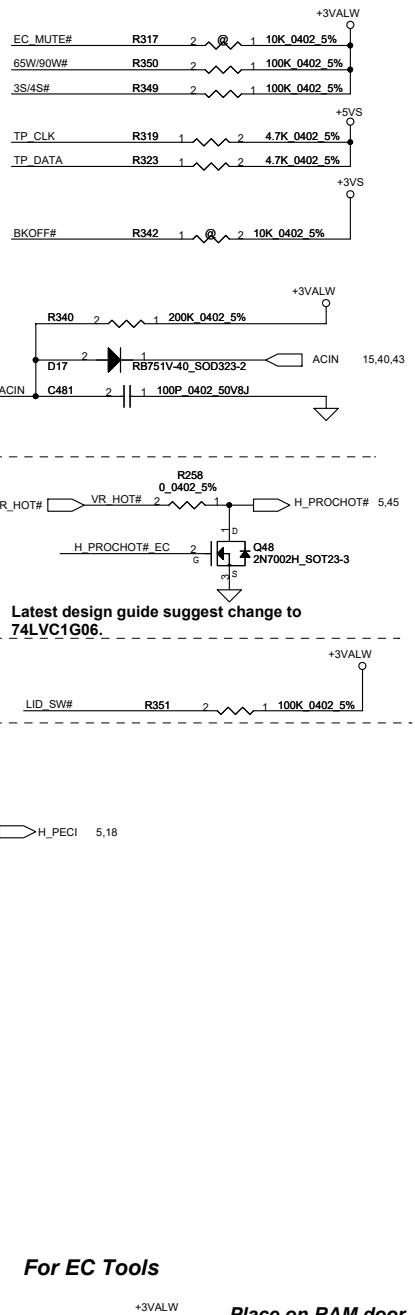
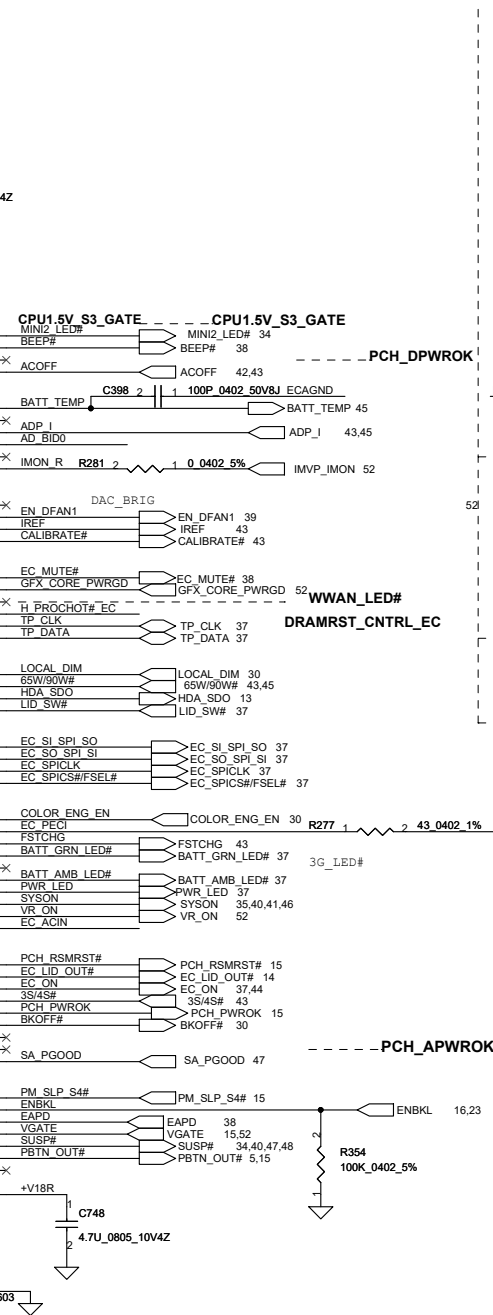
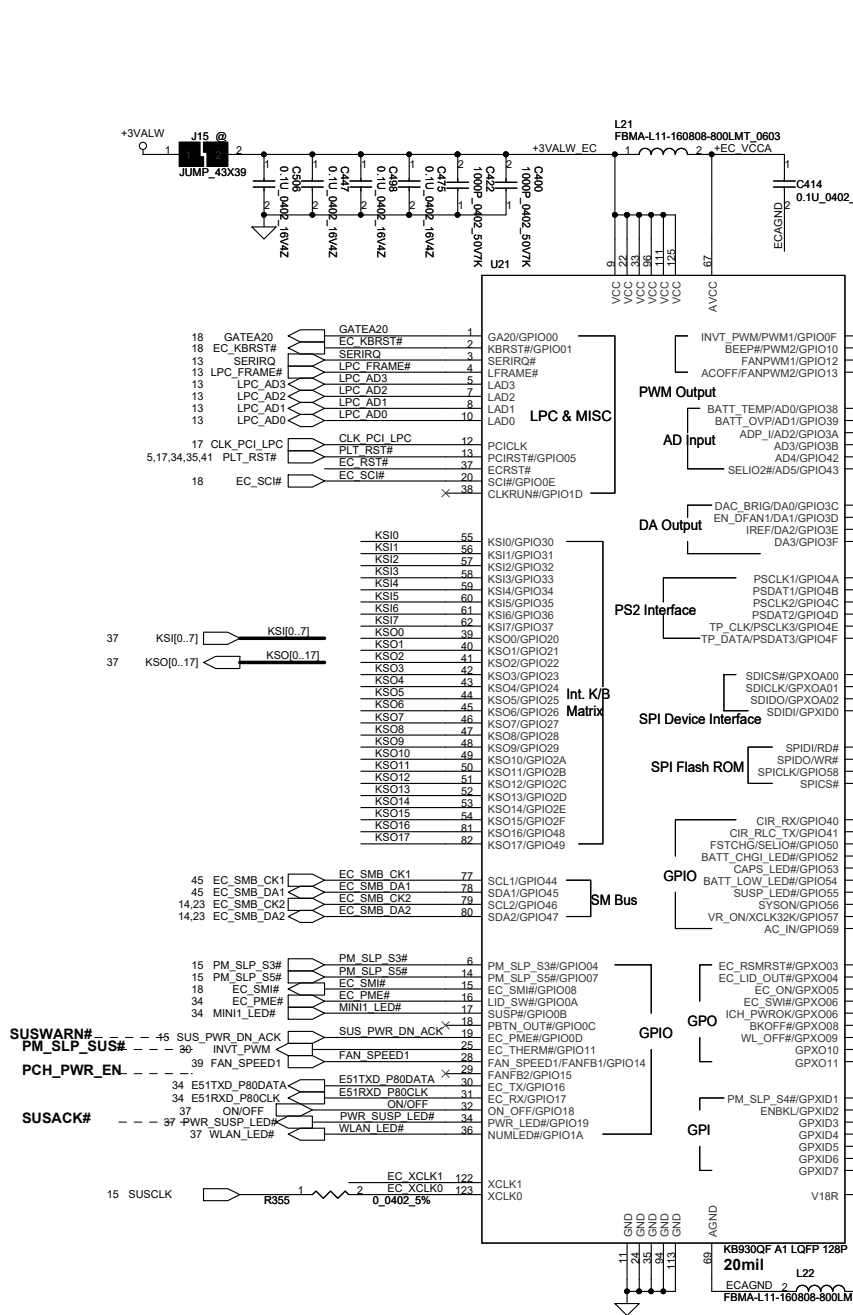
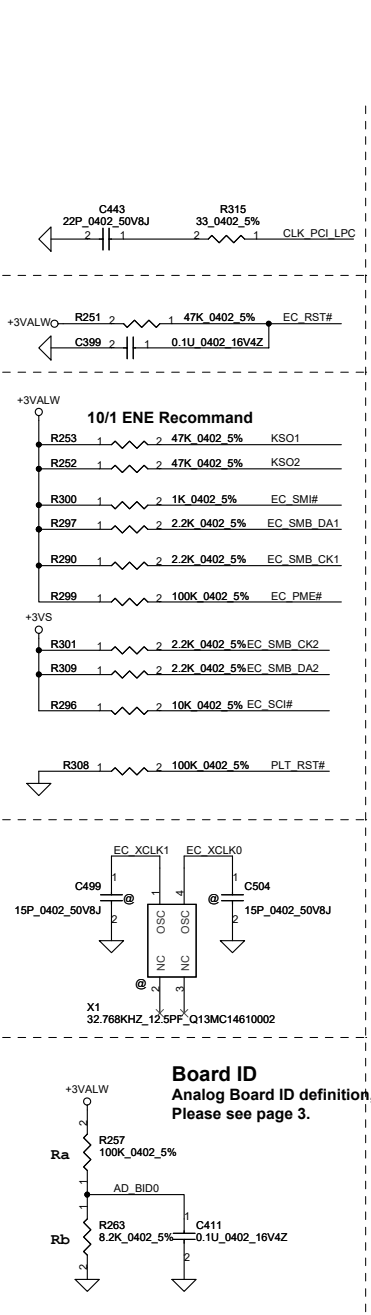
LS-6911P USB/B Conn. (USB2.0 SKU)

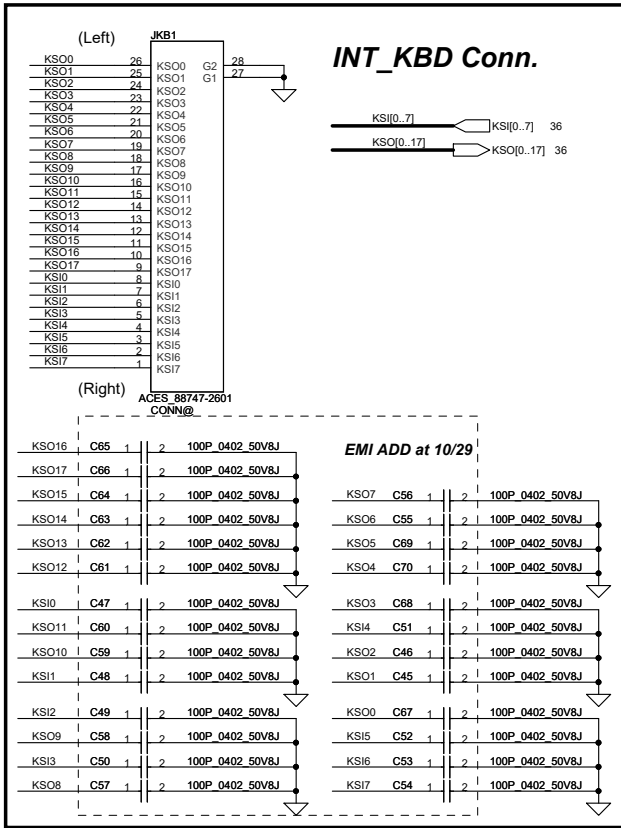
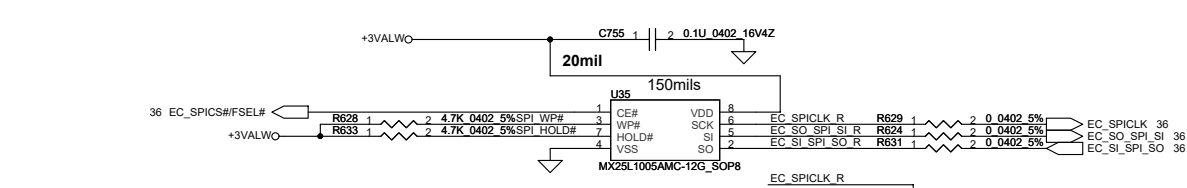


USB/B USB3.0 Conn.(USB3.0 SKU)

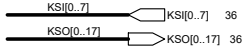
(Port 3)



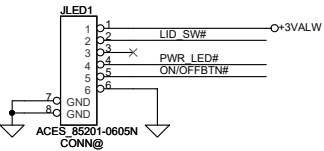




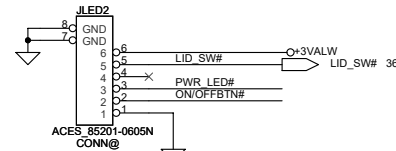
INT_KBD Conn.



LED/B P7YE0/P7YH0 LS-6913P



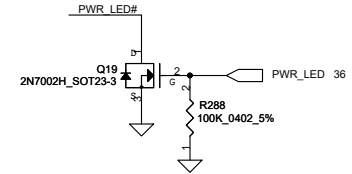
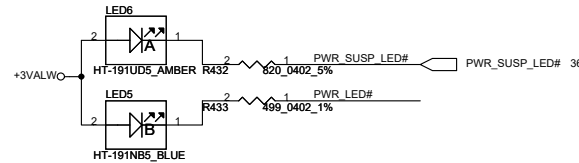
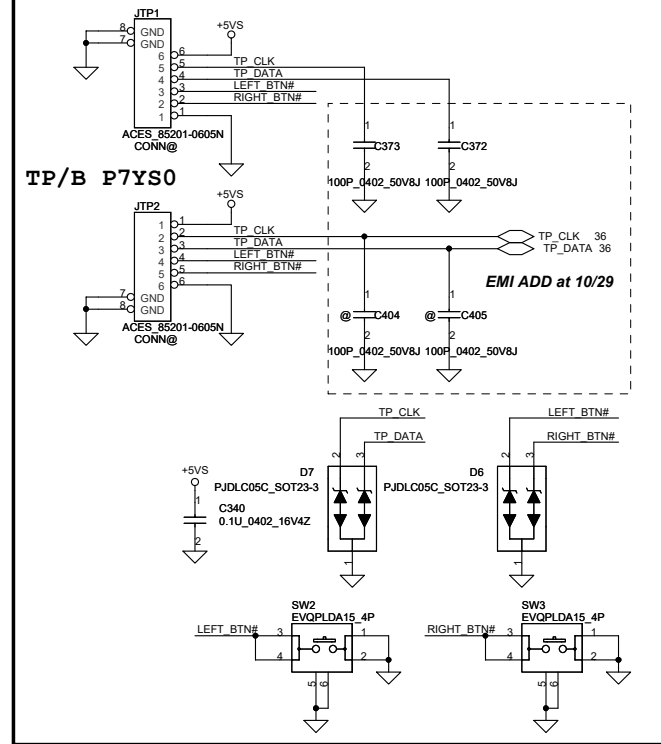
LED/B P7YS0 LS-6913P



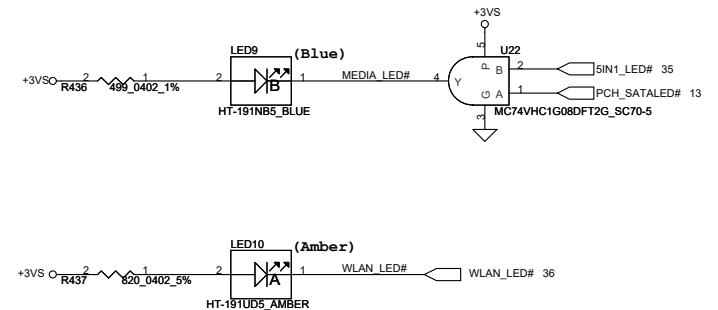
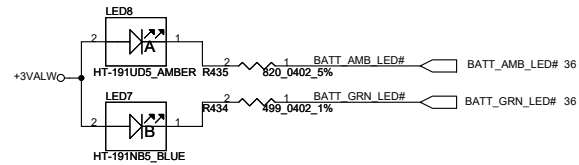
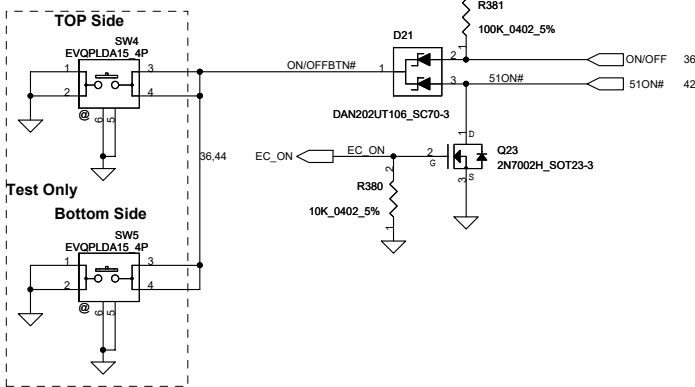
LED Status	Power/SUS		Battery		3G/WLAN	BlueTooth	ACIN
	ON	SUS	Full	Charge	3G	WLAN	
NEW70/80/90	Blue	Amber	Blue		Blue	Amber	

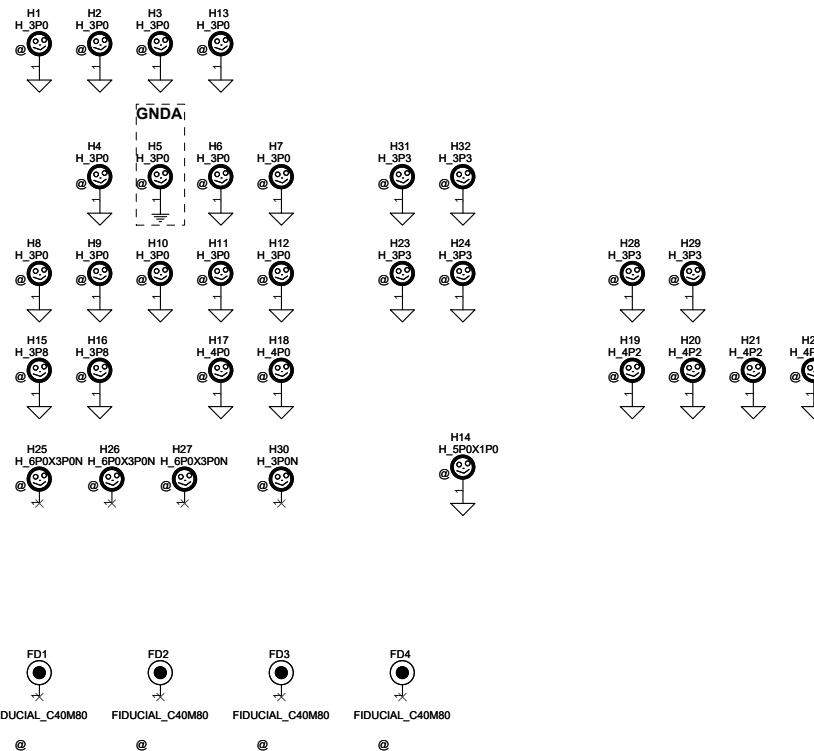
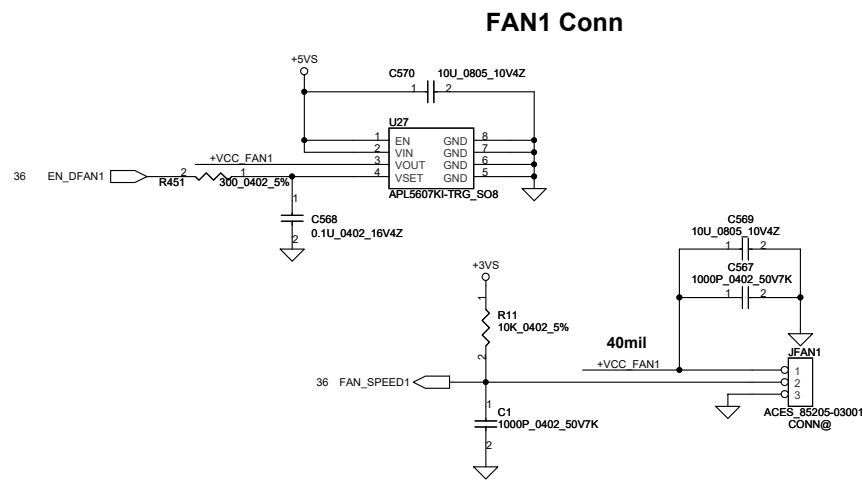
TP/B P7YE0/P7YH0

To TP/B Conn.

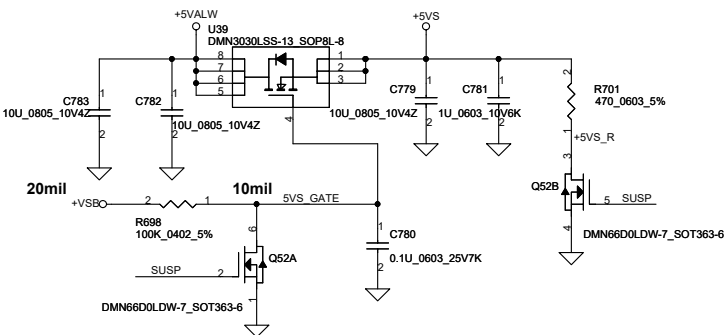


Power Button ON/OFF switch

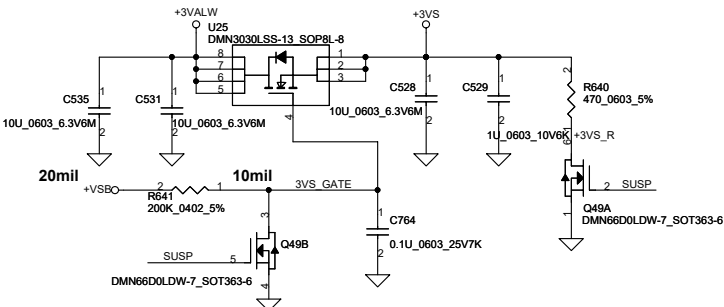




+5VALW TO +5VS

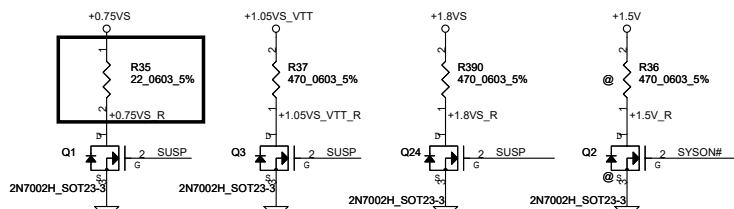
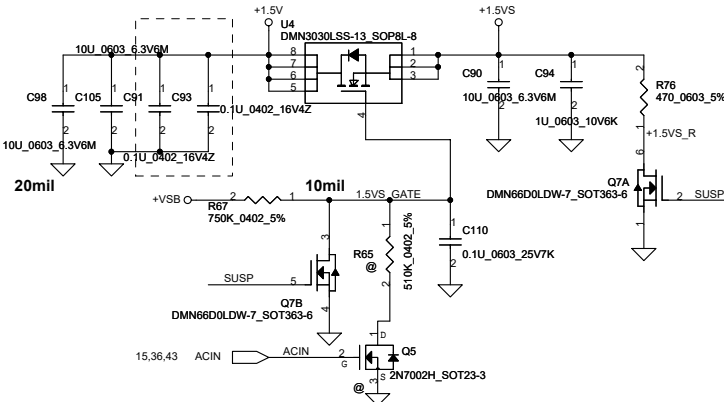


+3VALW TO +3VS



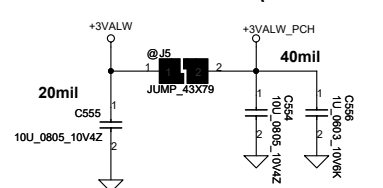
+1.5V to +1.5VS

1211 EMI ADD 0.1U close PJ5

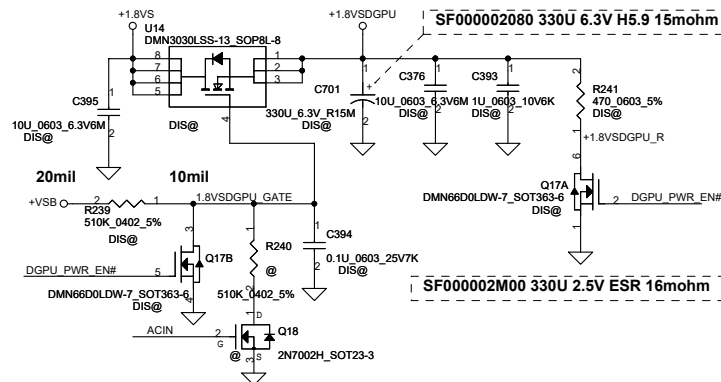


2009/08/14
CP_S3PowerReduction
WhitePaper_Rev0.9
0.75VS speed up discharge

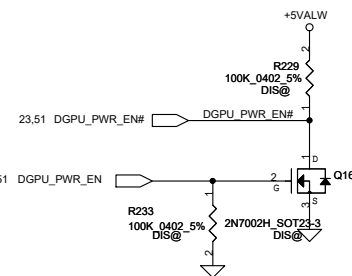
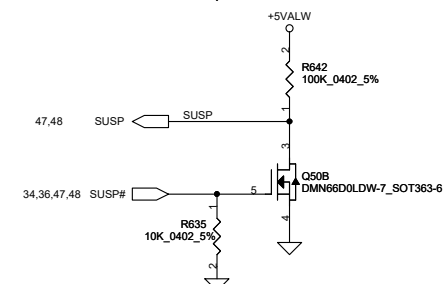
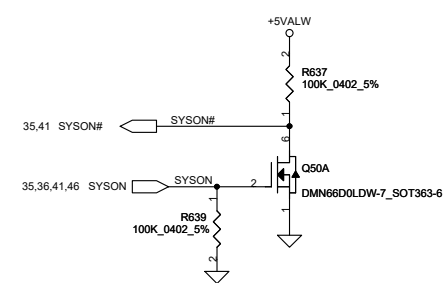
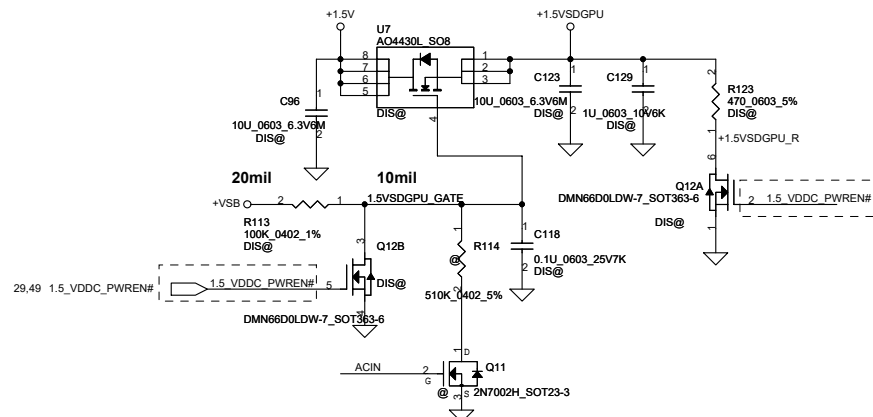
+3VALW TO +3VALW(PCH AUX Power)



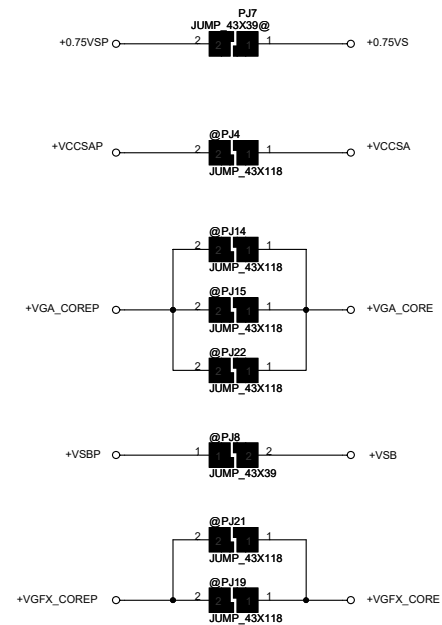
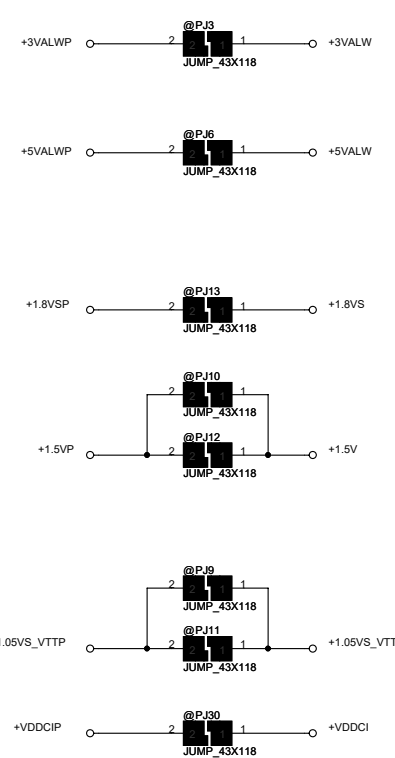
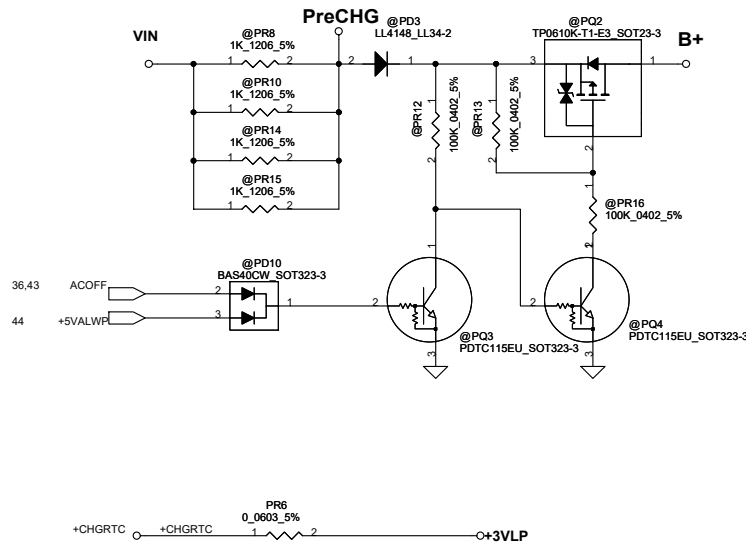
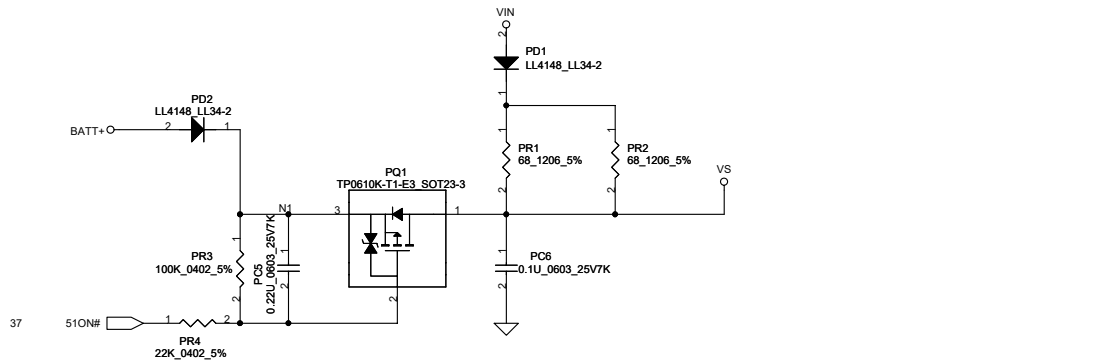
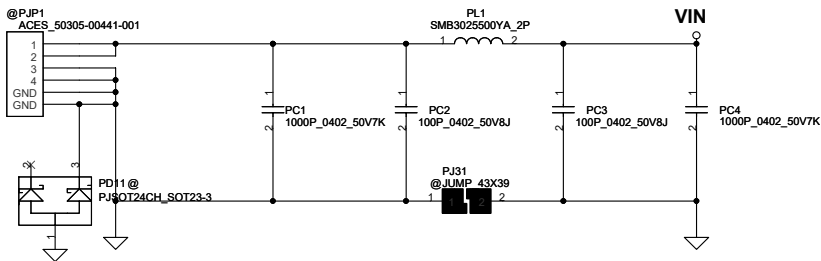
+1.8VS to +1.8VSDGPU for GPU



+1.5V to +1.5VSDGPU for GPU

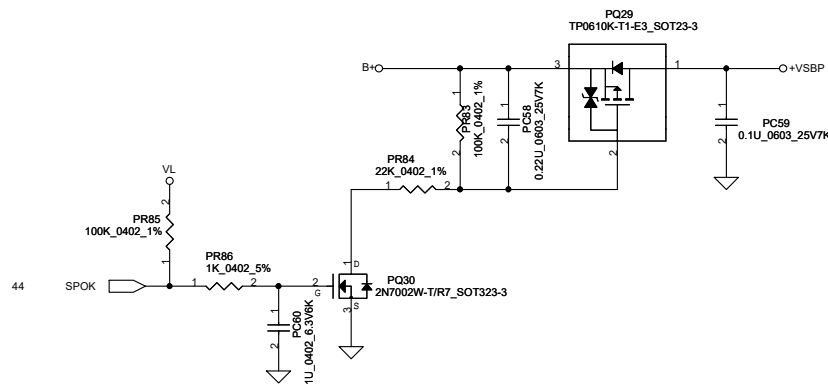
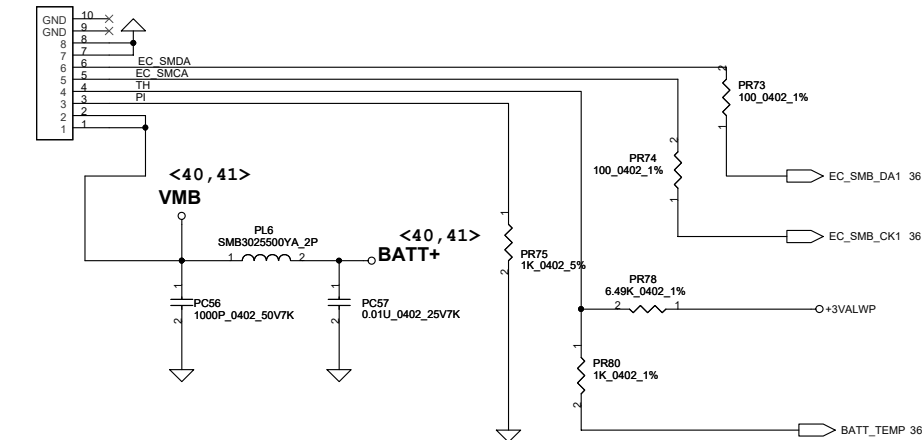


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				Document Number	4019A9
				Rev B	
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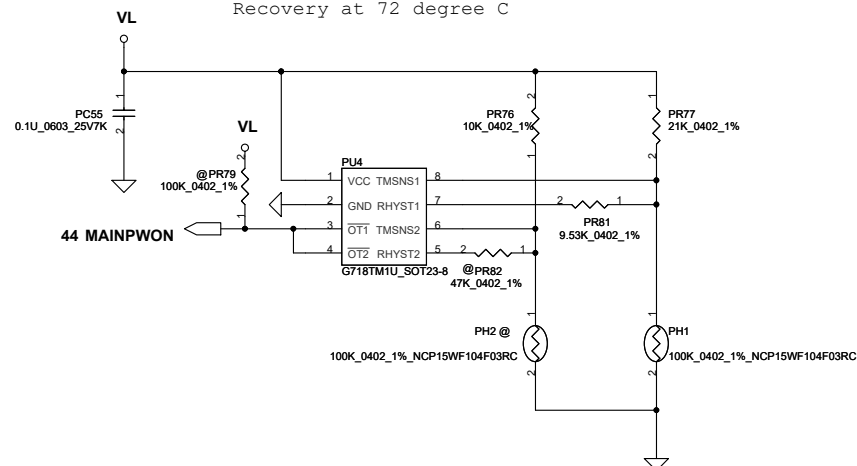


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						4019A9			
						Date: Tuesday, November 09, 2010		Sheet 42 of 60	

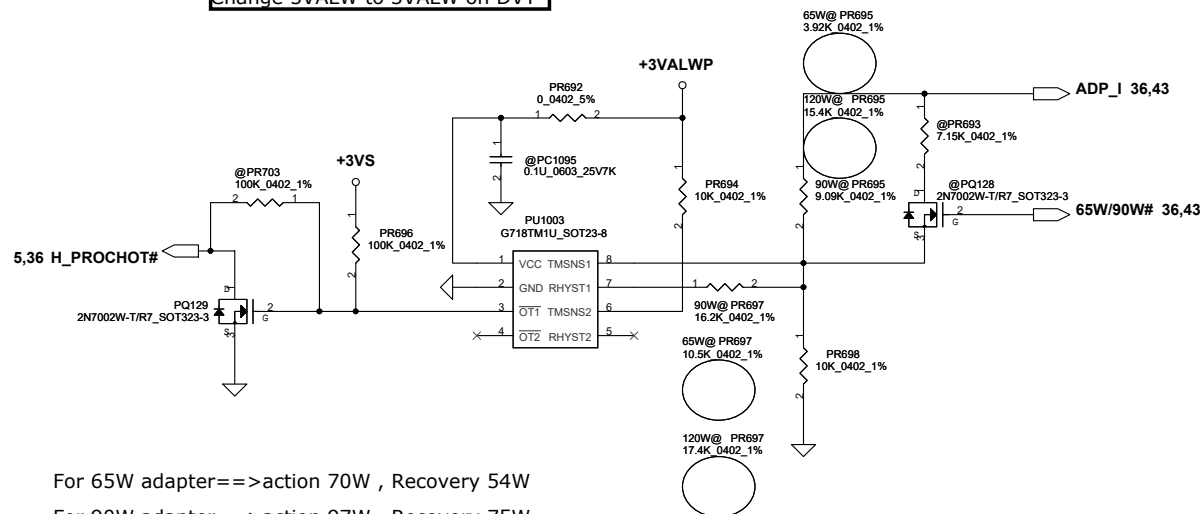
@PJ2
SUYIN_200275GR008G13GZR



PH1 under CPU botten side :
CPU thermal protection at 92 degree C
Recovery at 72 degree C



Change 5VALW to 3VALW on DVT



For 65W adapter==>action 70W , Recovery 54W
For 90W adapter==>action 97W , Recovery 75W
For 120W adapter==>action 135W , Recovery 100W

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						Part Number		4019A9		Rev B	
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						Custom					

35,36,40,41 SYSON

+5VALW

+5VALW

+1.5VP

+1.5VP
Ipeak=21.56A;1.2Ipeak=25.87A ;Imax=15.09A
Rton=267K, Fsw=298KHz ,Rdson=4.5~5.6mohm
Rtrip=16.5K
Iocp=25.97A~42.41A

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34,36,40,48 SUSP#

40,48 SUSP

1.8VSP
Ipeak=3.35A ; 1.2Ipeak=4.02 ; Imax=2.345A
Vout=0.6*(1+(20K/10K))=1.8V
-DVT-

Layout Note:
Place near V5FILT Pin

+VCCSAP
Ipeak=6A , Imax=4.2A, 1.2Ipeak=7.2A
DCR= 9 m(typ)~10 m(max)
Rlimit=12.1K,Rdson=14.5~17.9mohm
Iocp=7.24A~12.59A

VID[0]	VID[1]	VCCSA Vout	Require on 2011/ 2012 Required
0	0	0.9 V	Yes/Yes
0	1	0.8 V	Yes/Yes
1	1	0.75V	No/Yes
1	1	0.65V	No/Yes

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Note:Use VCCSA_SBI to switch High & Low Level for VID[1]

Ipeak
Granville(35W) 47A
Whistler(25W) 27A(VDDC+VDDCI)
Seymour(15W) 14.2A(VDDC+VDDCI)

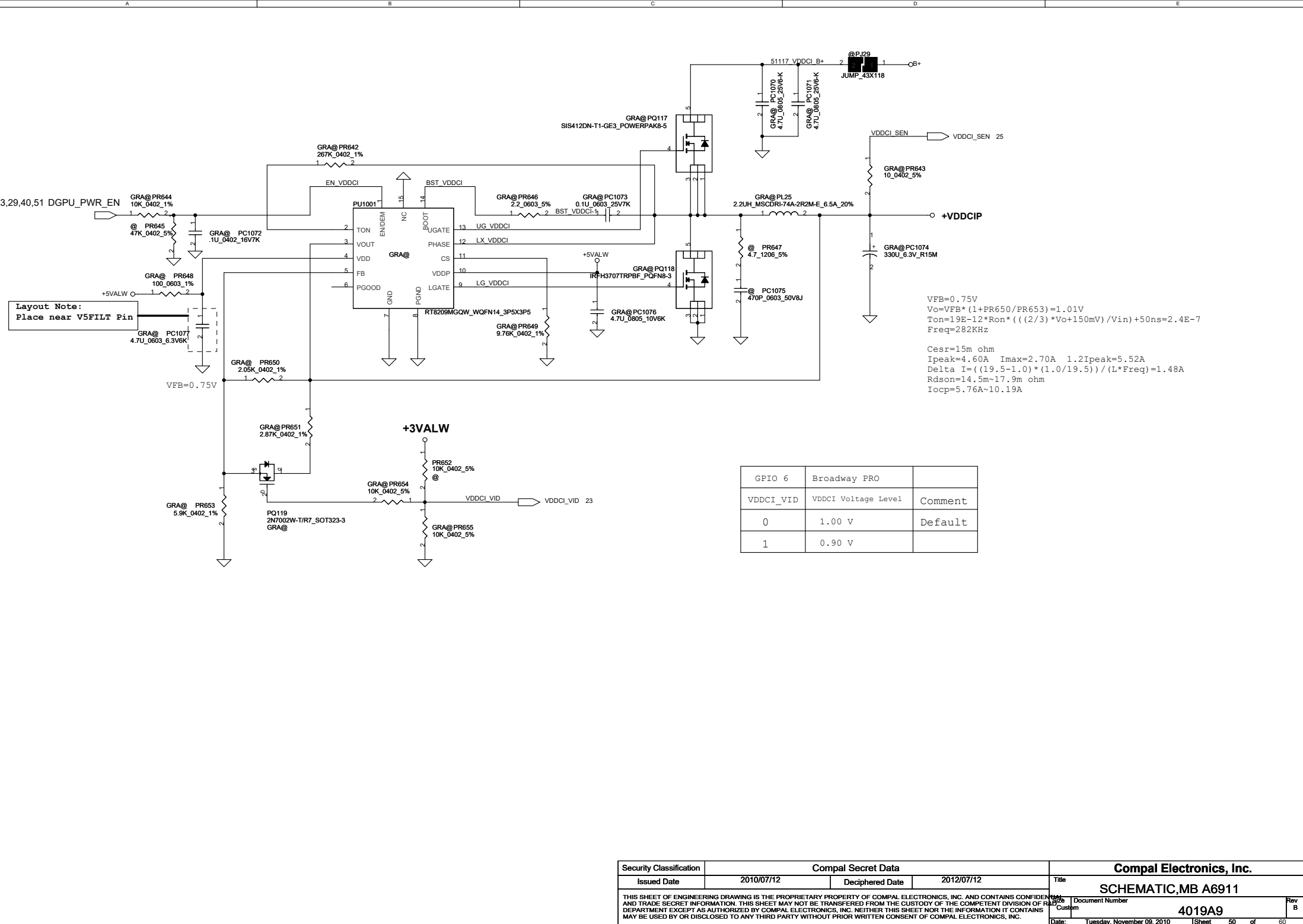
Switch freq. (RF pin setting)
47K ==>450KHz
100K ==>390KHz
200K ==>350KHz (Currently setting)
470K ==>300KHz

GPIO 15	GPIO 20	Whistler	Seymour	Granville
GPU_VID0	GPU_VID1	Core Voltage Level	Core Voltage Level	Core Voltage Level
1	1	0.85V	0.85V(0.855V)	0.90V
0	1	0.9V	0.9V(0.930V)	0.95V
1	0	1.00V	1.00V(1.025V)	1.00V
0	0		1.1V(1.100V)	1.05V

For Granville
1/2Delta I=4.05A
Vtrip=Rtrip*Itrip=64.9K*10uA=0.649V
Iocpmin=(Vtrip/8*Rdson)+1/2Delta
=(0.649V/(8*1.6m ohm))+4.502A
=50.7A+4.05A=54.75A

For Seymour
1/2Delta I=4.31A
Vtrip=40.2K*10uA=0.402V
Iocp=0.402V/(8*3.2m)+1/2Delta I
=15.70A+4.31A=20.01A

For Whistler
1/2Delta I=4.05A
Vtrip=36.5K*10uA=0.365V
Iocpmin=0.365V/(8*1.6m)+1/2Delta I=28.51A+4.05A
=32.56A

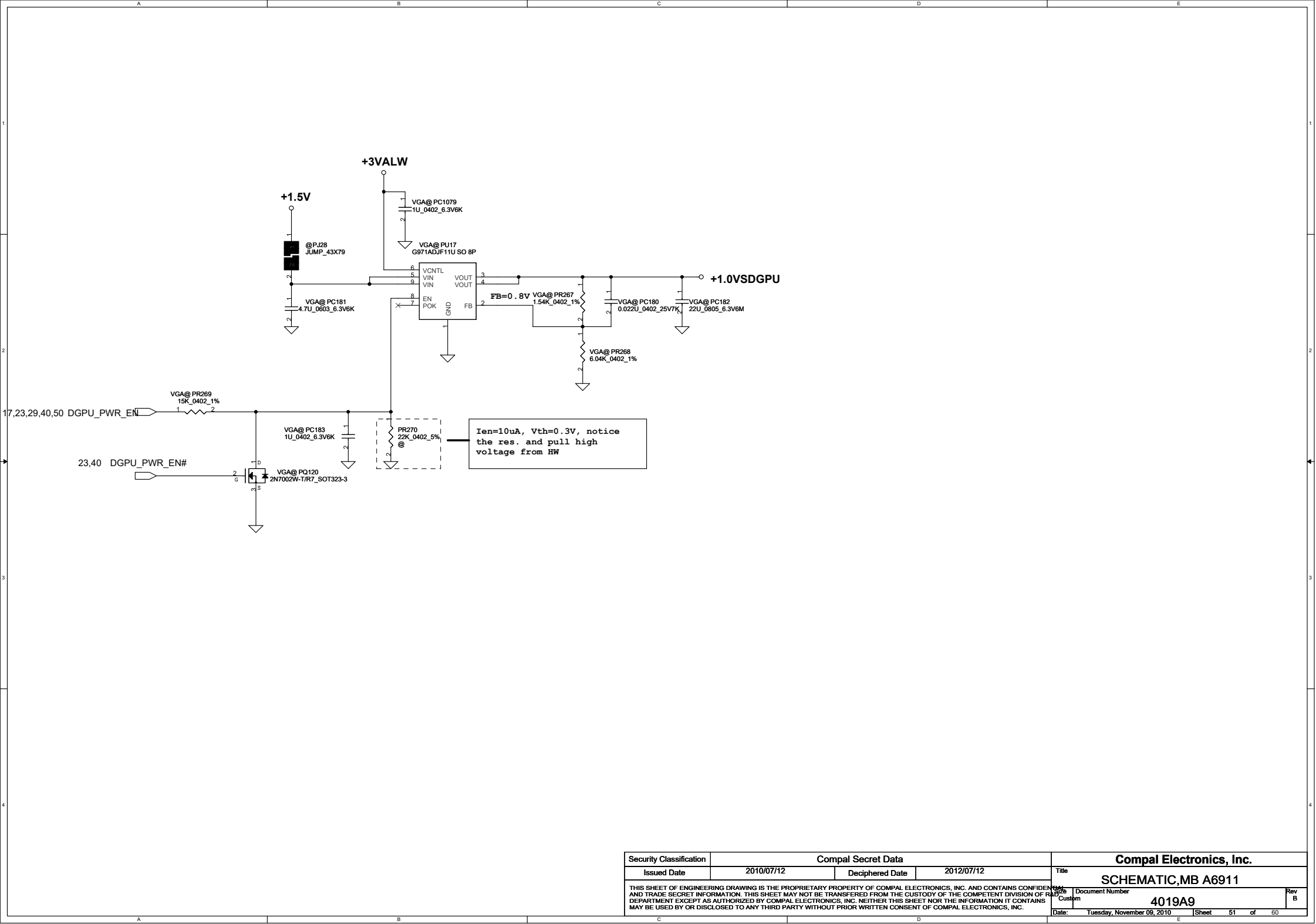


Layout Note:
Place near V5FILT Pin

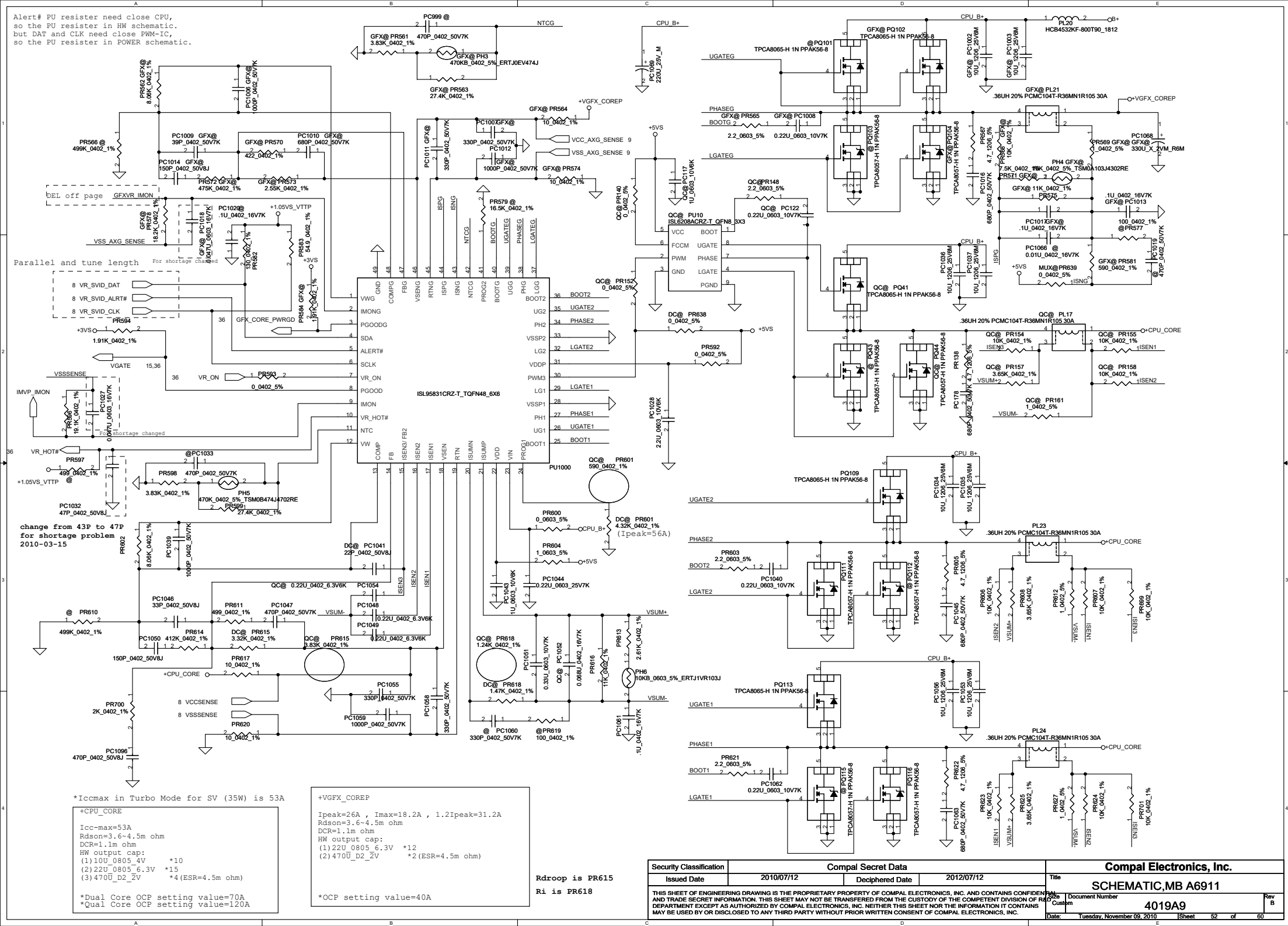
VFB=0.75V
Vo=VFB*(1+PR650/PR653)=1.01V
Ton=19E-12*Ron*((2/3)*Vo+150mV)/(Vin)+50ns=2.4E-7
Freq=282KHz

Cesr=15m ohm
Ipeak=4.60A Imax=2.70A 1.2Ipeak=5.52A
Delta I=((19.5-1.0)*(1.0/19.5))/(L*Freq)=1.48A
Rdson=14.5m~17.9m ohm
Iocp=5.76A~10.19A

GPIO 6	Broadway PRO	
VDDCI_VID	VDDCI Voltage Level	Comment
0	1.00 V	Default
1	0.90 V	



Alert# PU resister need close CPU,
so the PU resister in HW schematic.
but DAT and CLK need close PWM-IC,
so the PU resister in POWER schematic.



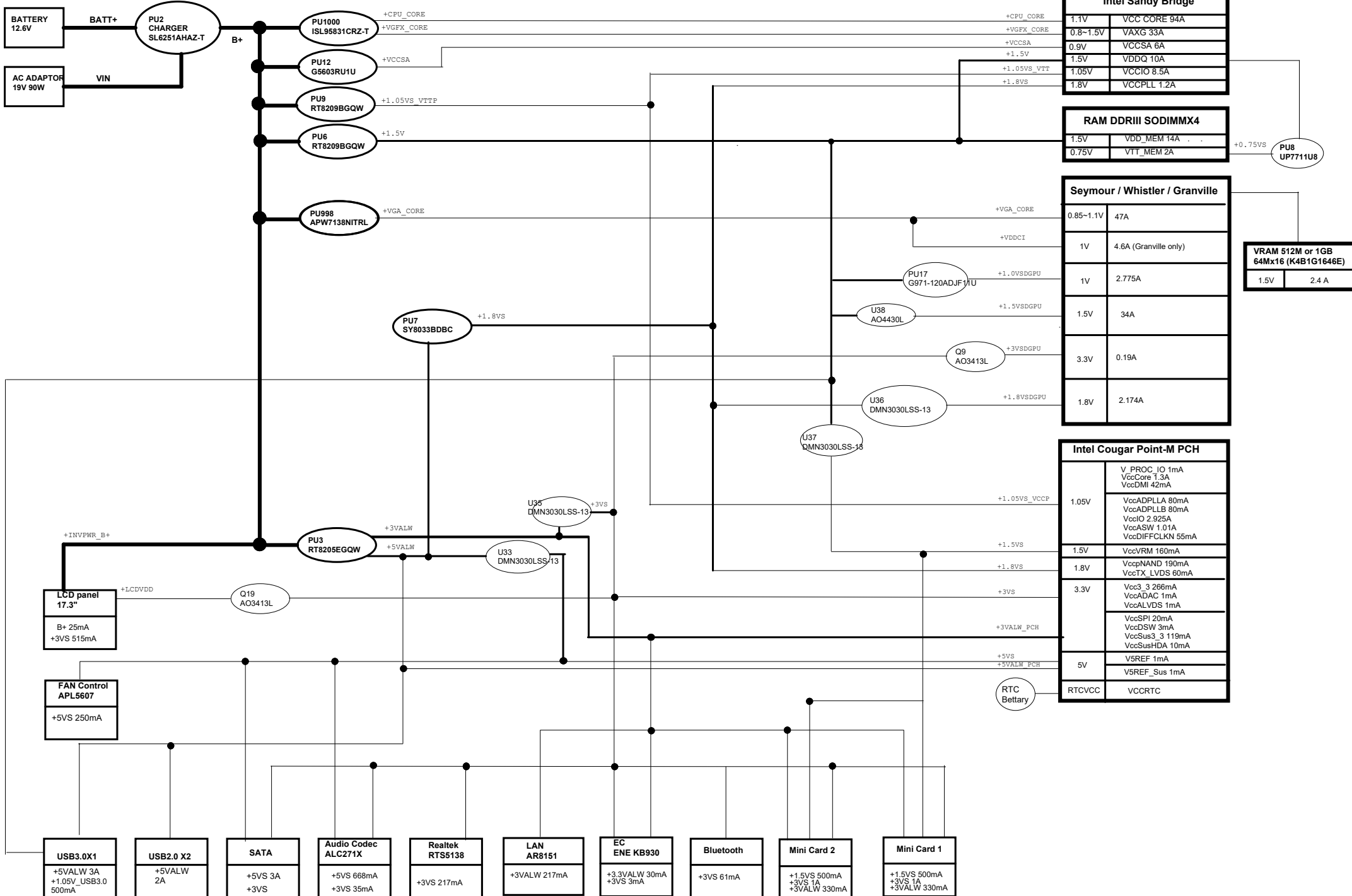
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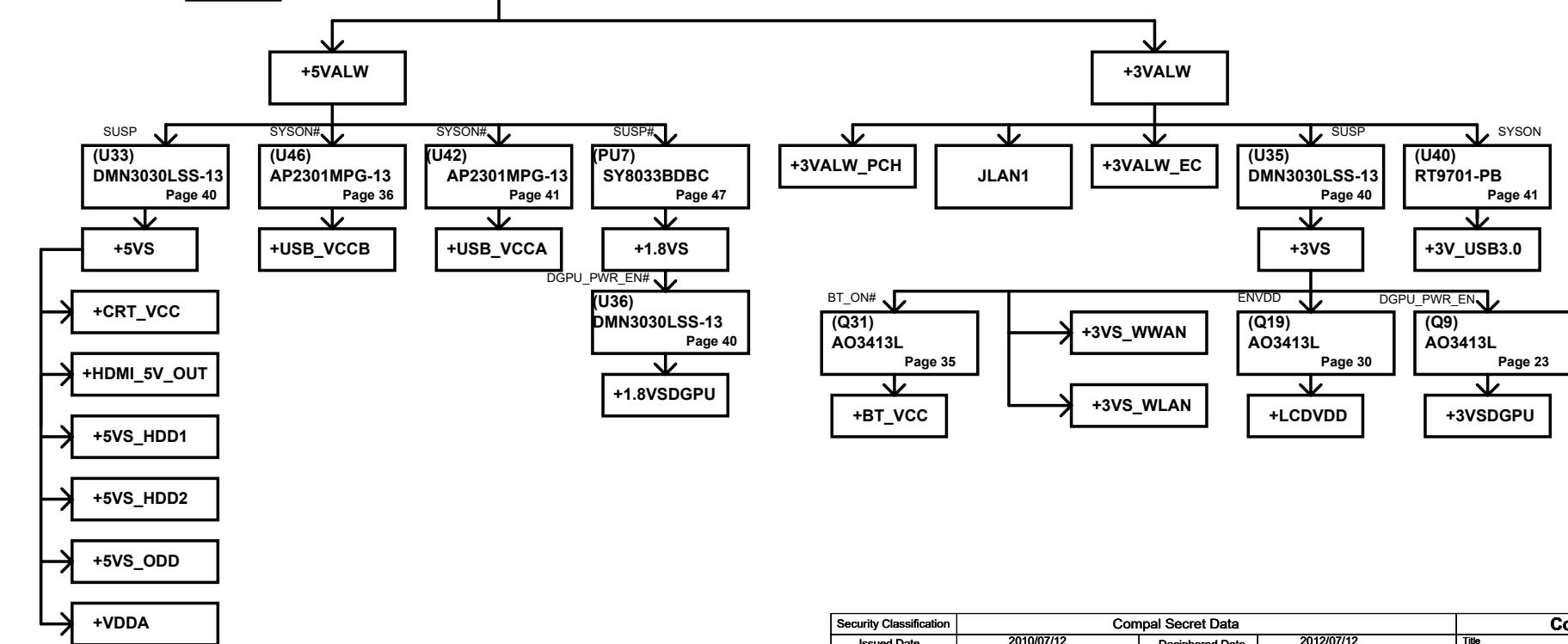
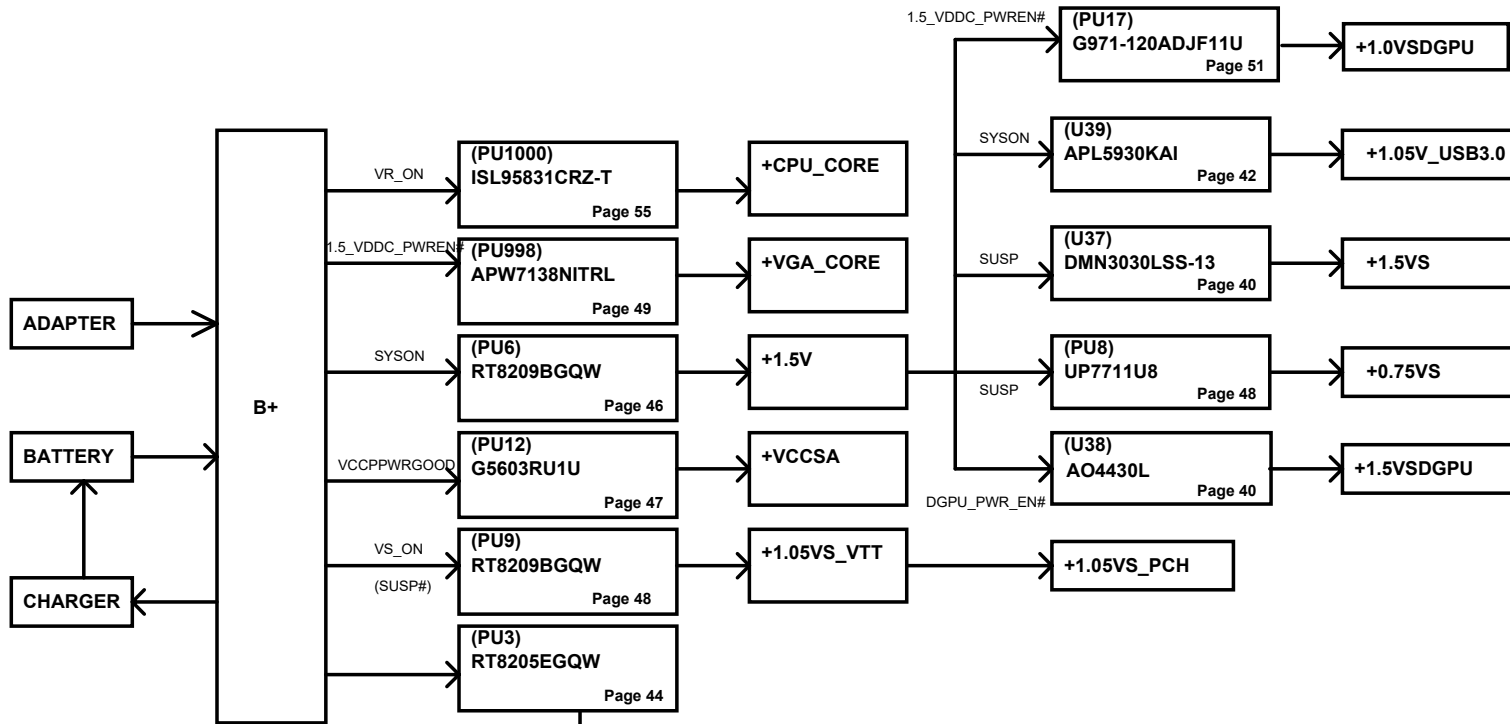
Version change list (P.I.R. List)

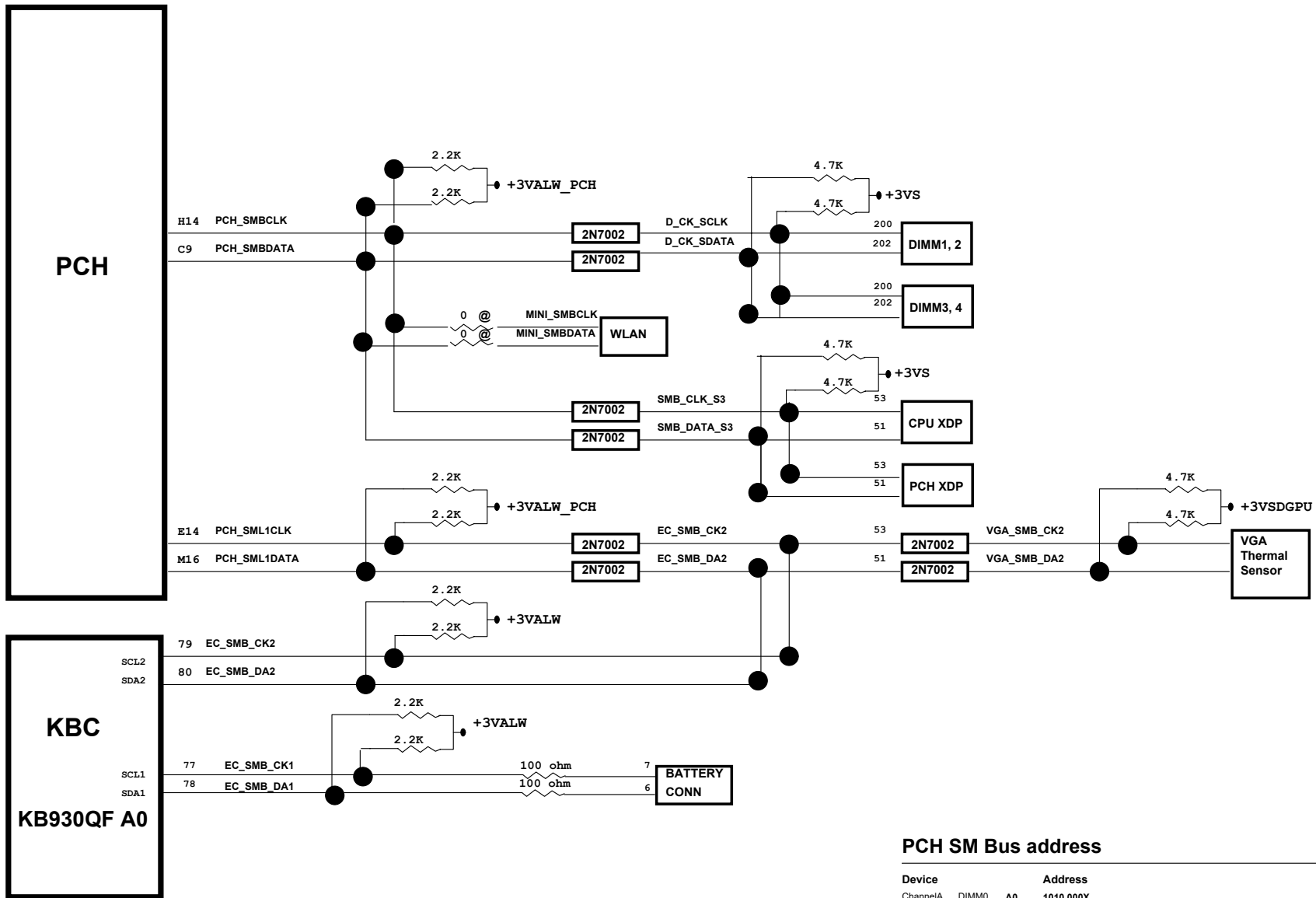
Page 1 of 1 for PWR

Item	Fixed Issue	Reason for change	Rev. PG#		Modify List	Date	Phase
1	HW increase 1.8V voltage.	HW need to increase 1.8V voltage.	0.1	47	Change PR106 from SD034100280 to SD034976180.	2010/09/23	DVT
2	VGA Granville OVP issue.	Because VGA has happened OVP issue in Granville SKU, that is caused by output capacitor too small. change PC1094 to SGA00004200 to solve it. PC1088 must remove.	0.1	49	Add PC1094 to SGA00004200 and delete PC1088 SF000002000.	2010/09/23	DVT
3	1.8V Power sequence adjust.	HW adjust 1.8V power sequence.	0.1	47	change PR104 from SD028100380 to SD028150380.	2010/09/23	DVT
4	0.75V Power sequence adjust.	HW adjust 0.75V power sequence.	0.1	48	Change PR127 from SD028150380 to SD034267380.	2010/09/23	DVT
5	adjust +1.05VS_VTT power sequence	HW adjust +1.05VS_VTT power sequence	0.1	48	Change PC99 from SE107475K80 to SE076104K80.	2010/09/23	DVT
6	adjust +VDDCI power sequence	HW adjust +VDDCI power sequence	0.1	50	Change PR644 from SD034301380 to SD034100280.	2010/09/23	DVT
7	HW request to delete PR103.	HW request to delete PR103.	0.2	47	Delete PR103 SD028100480.	2010/09/28	DVT
8	PR104 BOM error.	PR104 BOM error for power sequence.	0.2	47	Change PR104 from SD034150380 to SD034510380.	2010/09/28	DVT
9	PR669 BOM error for Seymour only.	PR669 BOM error for Seymour only.	0.2	49	Change PR669 from SD034681180 to SD034590180.	2010/09/28	DVT
10	To same as P5WE0 VCCSAP choke.	To same as P5WE0 VCCSAP choke.	0.2	47	Change PL10 from SH000009Q00 to SH00000M700.	2010/09/28	DVT
11	HW request to add PQ130 and PQ131 to speed up to 放电.	HW request to add PQ130 and PQ131 to speed up to 放电.	0.3	47 48	Add PQ130 and PQ131 SB000006800.	2010/10/05	DVT
12	Remove chargeable RTC battery.	We reserve chargeable RTC battery to prevent over heat issue, Thermal team result is pass, so remove chargeable RTC battery.	0.3	42	Delete PR691 SD013000080 Change PR6 from SD013560080 to SD013000080.	2010/10/05	DVT
13	Change PL4 and PL5 to TOKO new part.	Change PL4 and PL5 to TOKO new part.	0.3	44	Change PL4 and PL5 from SH000006J80 to SH00000MB00	2010/10/05	DVT
14	for ISN issue.	for ISN issue.	0.3	43	Add PL30 SH000009Q00 Delete PL28 SM010018210	2010/10/05	DVT
15	to same as P5WE0 choke.	to same as P5WE0 choke.	0.3	47	Change PL10 and PL11 from SH000009Q00 to SH00000F800	2010/10/05	DVT
16	for QC+25WGPU and QC+35W GPU change CP point.	Because Acer deine QC with 25W/35W GPU to be 120W SKU, change CP point to meet Acer request.	0.3	43	Delete PQ20 SB000006800. Delete PR48 SD034255180 Change PR22 from SD000001F00 to SD021100B80.	2010/10/05	DVT
17	for QC+25WGPU and QC+35W GPU change CP point.	Because Acer deine QC with 25W/35W GPU to be 120W SKU, change CP point to meet Acer request.	0.3	43	Change PR47 from SD034121280 to SD034100180 Change PR50 from SD034200280 to SD034511280	2010/10/05	DVT
18	Modify adapter throttling at turbo mode setting point.	Modify adapter throttling at turbo mode setting point.	0.3	45	Add PR695 SD034154280 Add PR697 SD034174280	2010/10/05	DVT
19	CPU Transient responds issue.	Change CPU transient responds RC time constant.	0.4	52	Add PC1052 SE000003J80. Add PC1096 SE071471J80. Add PR700 SD034200180.	2010/10/07	DVT
20	for ISN issue.	for ISN issue.	0.4	43	Change PL30 from SH000009Q00 to SH00000M700.	2010/10/07	DVT
21	Make BOM same as P5WE0.	Make BOM same as P5WE0.	0.4	52	Change PL21,PL23,PL24 from SH000005680 to SH00000HK00.	2010/10/07	DVT
22	BOM loss.	Because BOM Config loss 65@ and 90W@, so miss PR695 and PR697.	0.5	45	Add PR695 SD034909180 9.09K_0402_1% Add PR697 SD034162280 16.2K_0402_1%	2010/10/26	PVT
23	Modify CPU OCP.	Because original design is for 3 phase DC, now change to 2 phase DC, so modify OCP.	0.5	52	Change PR618 from SD034698080 to SD000009480	2010/10/26	PVT
24	Modify DC LL.	Because DC OCP was modified, must also update LL of DC.	0.5	52	Change PR615 from SD034215180 to SD034332180	2010/10/26	PVT

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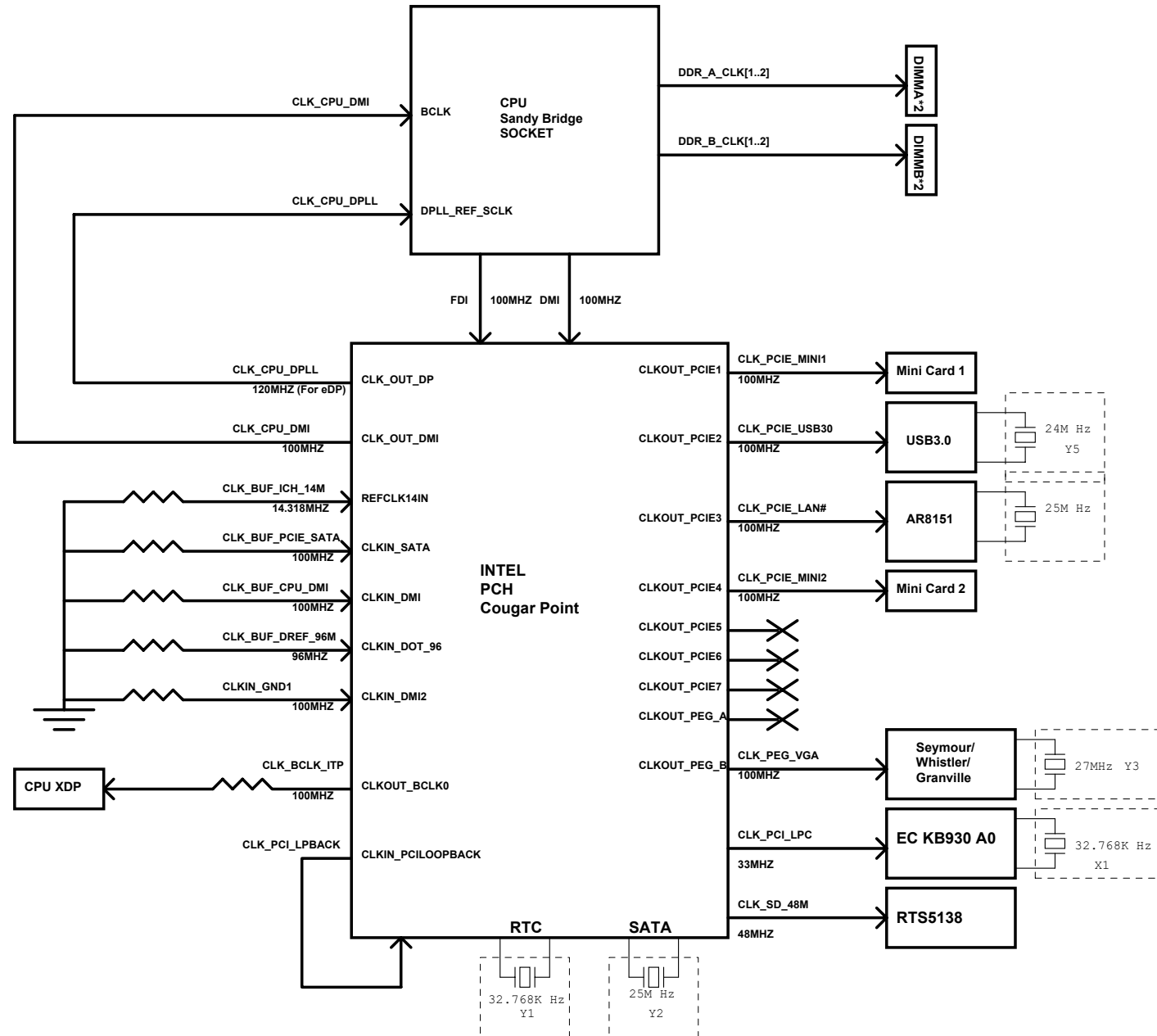


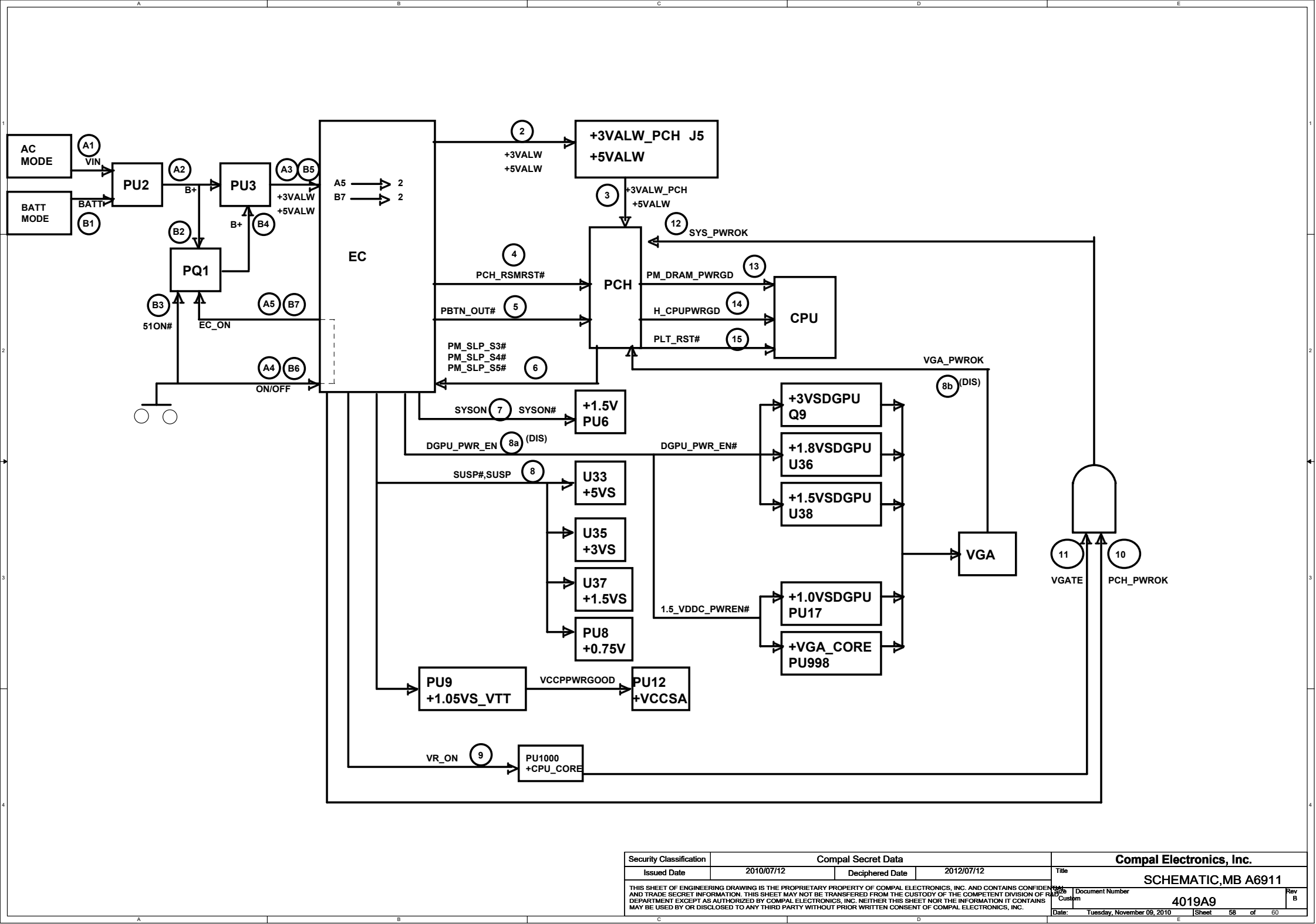




PCH SM Bus address

Device		Address	
ChannelA	DIMM0	A0	1010 000X
	DIMM1	A2	1010 001X
ChannelB	DIMM0	A4	1010 010X
	DIMM1	A6	1010 011X





PCB

LA-6911P MB Rev0: DA80000LC00
LA-6911P MB Rev1: DA80000LC10
LA-6911P MB with Small Board Rev1: DAZ
LA-6911P REV0 MB

VGA

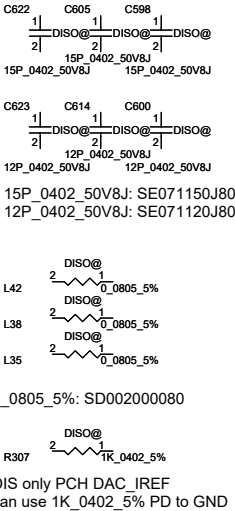
Granville PRO M2 A12:
SA00004C820(S IC 216-0769024 A12 GRANVILLE PRO ABO!)

WHISTLER PRO M2 A11:
SA00004C720(S IC 216-0810005 A11 WHISTLER PRO FCBGA 962P ABO !)

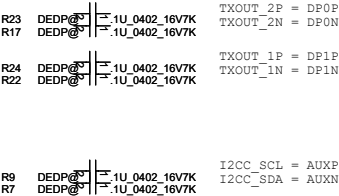
X76

- X761@ X76264BOL01 VRAM 512M SAM P7YE0
Samsung : SA000035720 (S IC D3 64MX16 K4W1G1646E-HC12 FBGA ABO!)
- X762@ X76264BOL02 VRAM 512M HYN P7YE0
Hynix : SA000032420 (S IC D3 64MX16 H5TQ1G63BFR-12C FBGA ABO!)
- X763@ X76264BOL03 VRAM 1G SAM P7YE0
Samsung : SA000035720 (S IC D3 64MX16 K4W1G1646E-HC12 FBGA ABO!)
- X764@ X76264BOL04 VRAM 1G HYN P7YE0
Hynix : SA000032420 (S IC D3 64MX16 H5TQ1G63BFR-12C FBGA ABO!)
- X765@ X76264BOL05 VRAM 2G HYN P7YE0
Hynix : SA00003VS10 (S IC D3 128M16 H5TQ2G63BFR-12C FBGA ABO!)
- X766@ X76264BOL06 VRAM 2G SAM P7YE0
Samsung : SA00003MQ60 (S IC D3 128M16 K4W2G1646C-HC12 FBGA ABO!)
- X767@ X76264BOL07 VRAM 1G SAM P7YE0
Samsung : SA00003MQ60 (S IC D3 128M16 K4W2G1646C-HC12 FBGA ABO!)
- X768@ X76264BOL08 VRAM 1G HYN P7YE0
Hynix : SA00003VS10 (S IC D3 128M16 H5TQ2G63BFR-12C FBGA ABO!)

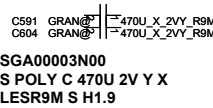
CRT Option Components



DIS EDP Option Components



Granville VGA_CORE CAP Option



EC susclk/crystal Option Components



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